MSU RTC Team
April 27, 2012
MSU – Payload 04

Dr. Gregory Guzik
LSU HASP Program

Re: Monthly Status Report – April 2012

The MSU RTC HASP team focused work in two main areas in April – FPGA CCA schematic capture and system design, and continued thermal analysis of the payload. The design process for an FPGA circuit board is highly iterative. The FPGA architect and the FPGA board designer must work together to find a pin assignment arrangement that both allows successful placement and routing internal to the FPGA and minimizes routing complexity on the circuit board. The circuit design process and schematic capture for the FPGA CCA are nearly complete. Our second priority carries over from our earlier thermal analysis results which indicated that the payload may reach internal temperatures of +125 ˚C, which is unacceptably high. Lizi, our team's mechanical engineer, resigned due to scheduling conflicts. The other team members are working to pick up where she left off, and have been working to fully understand the thermal heating problem in order to arrive at an effective heat dissipation solution. We understand that at altitude we cannot rely on convective cooling to move heat away from the chips due to the low atmospheric pressure. We must use a combination of conductive and radiative heat transfer to move heat away from the chips and subsequently radiate the heat away from the payload. This can be accomplished by affixing thermal conductors to the chips that generate excessive heat and routing these conductors to a high-emissivity material mounted in a nadir aperture shielded from direct exposure to solar irradiance. We found that reducing our insulation layer thickness slightly and using a thin, painted aluminum enclosure (rather than white polycarbonate) significantly lowered the internal temperature (~+77 ˚C during float). This temperature is within our operating range and we are continuing to develop a better understanding of the thermal behavior of the payload. We have found access to a small thermal chamber which should allow us to test the payload up to +60 ˚C, and are working to find a vacuum chamber for testing in low pressure conditions prior to integration.

Justin Hogan – Justin continued work on the FPGA CCA schematic capture and PCB layout. The majority of the FPGA circuitry has been captured and a design review prior to fabrication is expected in the next week. Justin picked up the thermal analysis work in addition to PCB design.

Raymond Weber – Raymond finalized the control FPGA architecture and is awaiting FPGA CCA completion to begin testing. He generated the circuit schematic symbols for both FPGAs, performed pin selection to minimize PCB routing complexity and is helping with thermal analysis using a tool (Hyperlynx Thermal) which allows importation of PCB designs for thermal simulation. This tool will give us board-level temperatures under customizable operating

conditions (including atmospheric pressure, enclosure dimensions and material, heat sink components, thermal properties of chips and FR4 PCB material, etc.).

Todd Buerkle – Todd assisted with the preliminary Payload Specification and Integration Plan and continued the hand-off process of the radiation sensors and amplifier circuits as he prepares for graduation.

Jennifer Hane – Jennifer is also graduating and she has been debriefing Raymond on the operation, design, development and maintenance of the partially reconfigurable computer architecture and the corresponding design tools.

Lizi Clem – Resigned.

Adrien Lambert – Adrien is a mechanical engineer and is reviewing our thermal calculations. Additionally, his independent research involves the mechanical characterization of our computer/sensor stack architecture. This work is valuable in understanding the resonant modes of our stack and has provided valuable insight into mounting our stack within a payload.

Issues encountered during payload design and development

Thermal analysis and PCB design are the major design foci. We made a change to the control FPGA to move to a larger device with more logic resources. This change required a footprint change on the PCB and re-routing of several I/O lines.

Mechanical engineer resigned, looking for a replacement for the summer.

Milestones Achieved

- Majority of FPGA schematic capture completed.
- Received mounting plate.
- FPGA pinouts selected

Current team members and leaders

Name	Team Role	E-mail	Phone
Dr. Brock LaMeres	Principal Faculty Advisor	lameres@ece.montana.edu	(406) 994-5987
Dr. Todd Kaiser	Faculty Advisor	tjkaiser@ee.montana.edu	(406) 994-7276
Justin Hogan	Principal Team Lead	justin.hogan@msu.montana.edu	(505) 977-3844
Ray Weber	Principal Team	raymond.weber@msu.montana.edu	(406) 994-5975
Jennifer Hane	Team Member	jennifer.hane@msu.montana.edu	
Todd Buerkle	Team Member	toddbuerkle@gmail.com	
Adrien Lambert	Team Member	adrien.lambert@msu.montana.edu	