HASP Student Payload Application for 2018

Payload Title: Stratospheric Spectropolarimeter Gamma-X (SSGX)

Institution: American River College (USA), University of Coimbra (Portugal), INAF-IASF Bologna (Italy)

Payload Class (Enter SMALL, or LARGE): LARGE

Submit Date: December 15, 2017

Project Abstract: Among the last frontiers of astronomy are the polarization measurements of x- and γ-rays, emitted from phenomena as diverse as γ-ray bursts, pulsars, and active galactic nuclei. Our payload consists of a 4x4 pixel CdTe prototype developed to characterize background radiation in the 20-1000 keV energy range. Measuring double events is essential in determining Compton photons' new direction and therefore the polarization direction. The SSGX payload features both the CACTμS detection unit which previously launched from Italy in 2002 (recording single events), and an innovative electronic data collection system designed by ARC's Physics and Astronomy Club. The Data Acquisition/Integrated Storage Interface (DAISI) is responsible for sampling detector analog voltages, supplying required voltages, monitoring system operation, regulating electronics temperature, responding to remote communication, and the continuous recording of acquired data as well as system status to permanent storage. While this may not be the "sexiest" of experiments, it is crucial to develop reliable calibration data for future instruments; further, this project provisions hands-on experience for undergraduates within an international collaboration. Our goal is thus to obtain, for the first time, a fine measurement of all background components (single, double, and multiple events) that can deteriorate a γ-ray polarimeter response in space.

Team Name: ARC Physics & Astronomy Club

Team or Project Website: https://github.com/Sternzeug/DAISI

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I. Payload Description

1.1 Scientific Background

High-energy astrophysics polarimetry has experienced only modest exploration due to the high degree of complexity -- not only in detection methodology and the related electronic signaling and processing systems, but also due to the specific constraints in the targets of interest; celestial γ-rays can only be observed from either space, sounding rockets, or via high-altitude balloon missions. To date, x- and γ-ray emissions have been studied almost exclusively through spectral and timing variability analysis, or by using imaging techniques based on coded mask cameras or telescopes equipped with high-efficiency focal plane detectors.

By measuring the polarization angle and degree of linear polarization of the detected emissions, the number of observational parameters is increased by two, thereby enhancing discrimination between different models that characterize the same object. Polarimetric observations can provide important information about the geometry, magnetic field, composition and emission mechanisms of astrophysical sources. Polarization and degree are typically independent parameters, providing geometric information about a specific object, which is decoupled from its physical processes; this enables improvements in modeling, independent of physical principles. Polarized x- and γ-ray emissions are expected from a wide variety of sources, including pulsars, solar flares, active galactic nuclei, galactic black holes, and γ-ray bursts [1].

Polarization in the x-ray (<10 keV) domain has been observed since as early as the 1970s, as exemplified by the Aerobee-350 sounding rocket flight (from NASA's Wallops Island) and by OSO-8's (Orbiting Solar Observatory) polarimeter -- each of which measured the Crab Nebula polarization [2,3]. Progress in γ-ray astronomy has been more difficult to achieve. Although further space-dedicated polarimeters have been proposed [4-7], the first conclusive polarimetric measurements in the soft γ-ray domain (100 keV - 1 MeV) was performed by the INTEGRAL (INTErnational Gamma-Ray Astrophysics Laboratory) mission, launched in 2002 [8,9]. These observations of the Crab Pulsar and the stellar black hole Cygnus X-1 [10-12], were made using INTEGRAL's instruments SPI (Spectrometer on INTEGRAL) and IBIS (Imager on Board the INTEGRAL Satellite).

1.2 Polarimetry Fundamentals and Simulation

1.2.1 Polarization Fundamentals

The importance of polarimetry is today largely recognized within the high-energy astrophysical community, thus the next generation of space missions aims to provide polarimetric observations of the high-energy Universe. This is indeed the case for the high-energy (300 keV - 3 GeV) space mission proposal asserted by the e-ASTROGAM Consortium for the fifth medium-sized European Space Agency Cosmic Vision program (M5). Polarimetry is in fact among the main objectives for this mission proposal [13]. In the framework of the development of e-ASTROGAM's focal plane optimized for polarimetry (several detector types are being considered, such as Si and Ge), a CdTe polarimeter prototype was tested under a partially polarized beam generated by Compton scattering on a target, when irradiated by a ^{22}Na (511 keV) radioactive source.

The balloon experiment herein proposed represents a constituent element of a larger project that includes vast polarimetry simulations with GEANT4 and a series of experiments carried out at the ESRF (European Synchrotron Radiation Facility) under monochromatic-polarized beams between 100 and 750 keV [14-19]. In this energy band, polarimetry is based in Compton Scattering.

The polarimetric performance of a focal plane detector is determined by the fundamental concepts associated with polarized Compton interactions. The Compton scattering of polarized photons generates non-uniformity in the azimuthal angular distribution. After undergoing Compton scattering, the polarized photon's new direction depends on the orientation of its polarization before the interaction. If the polarized photon undergoes a new interaction inside the detector, the statistical distribution of the relative positions of the two interactions (double event) allows for inference of the degree and polarization direction of the incident radiation. The Klein-Nishina cross-section for linearly polarized photons gives us an azimuthal dependency for the scattered photons:

$$\frac{d\sigma}{d\Omega} = \frac{r_0^2}{2}\left(\frac{E'}{E}\right)^2\left[\frac{E'}{E} + \frac{E}{E'} - 2\sin^2\theta\cos^2\varphi\right] \tag{1}$$

Where $\mathbf{r_0}$ is the classical electron radius, **E** and **E'** are the energies of the incoming and outgoing photons (respectively), $\boldsymbol{\Theta}$ the angle of the scattered photon, and $\boldsymbol{\varphi}$ is the angle between the scattering plane (defined by the incoming and outgoing photon directions) and incident polarization plane (defined by the polarization direction and the direction of the incoming photon). As can be seen from (1), after fixing all other parameters the probability of interaction varies with the azimuthal angle $\boldsymbol{\varphi}$ and its maximum and minimum arises for orthogonal directions. For $\boldsymbol{\varphi}$= 0° the cross-section reaches a minimum and for $\boldsymbol{\varphi}$ = 90° the cross-section reaches a maximum. However, this relative difference is maximized for an angle $\boldsymbol{\Theta}_M$, dependent on the incident photon energy. For soft γ- and hard X-rays (100 keV - 1 MeV) the $\boldsymbol{\Theta}_M$ value is about 90°.

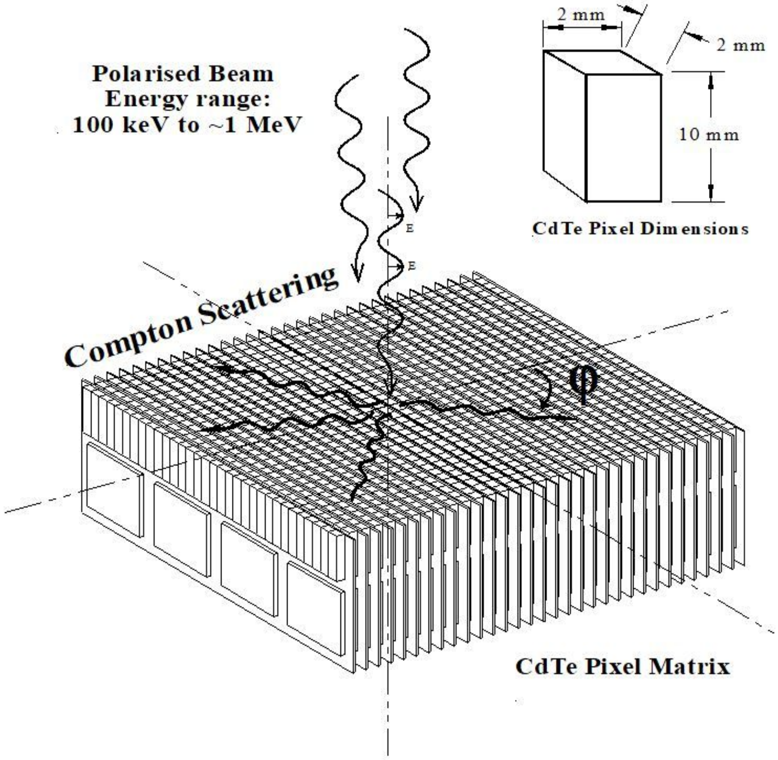

Fig. 1 - Compton scattering in a CdTe pixel matrix. Illustration taken from [14].

The polarimetric performance of an instrument can be evaluated by analyzing the distribution of double events through the polarimetric modulation factor, Q. This is obtained by integrating the Compton polarimetric differential cross-section formula given by (1) over the solid angles defined by the physical geometry of the detection plane, and for a pixel detector can be written as:

$$Q = \frac{N_x - N_y}{N_x + N_y} \tag{2}$$

Here we obtain Q through the number of double events, N_x and N_y, integrated over two orthogonal directions (x and y) defined over the detector plane.

1.2.2 Polarization Simulations

In order to predict the CdTe polarimetric performance, researchers typically develop Monte Carlo codes based on GEANT4 library modules in order to simulate the detector behaviour under polarized and unpolarized photon fluxes. This is a prerequisite for ulterior comparison with flight data.

GEANT4, an acronym for GEometry ANd Tracking, is a software toolkit used for the simulating the passage of particles through matter. Its areas of application include high energy, nuclear and accelerator physics, as well as studies in medical and space sciences.

Simulations usually focus on two main aspects: physical and geometric. The physical concepts involve electromagnetic interactions, particularly with respect to polarized Compton scattering. The detection geometry concepts focus on aspects such as beam characteristics, detection plane, and read-out geometry. A complete simulation must, therefore, include factors such as the energy of the beams, their inclination angles, efficiency of the detectors, etc..

Clarifying further the content of Fig. 1, the illustration below shows the scattering probability diagram from the Klein-Nishina (KN) equation (1) as a function of the azimuthal angle, **φ**. It also shows a generic Compton scattering event, where the incoming photon is represented in blue and the scattered photon is represented in red.

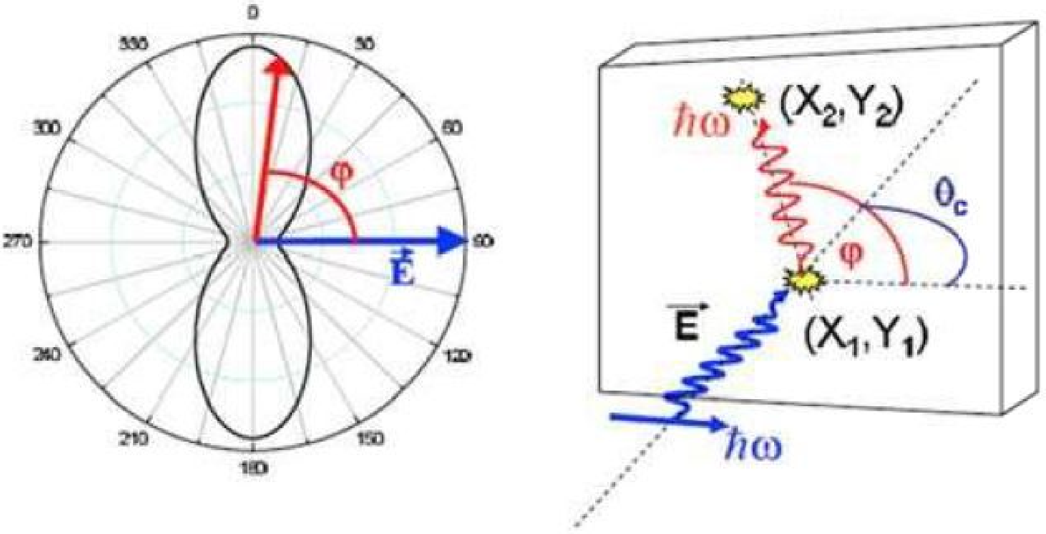

Fig. 2 - On the left, the scattering probability diagram from the KN equation. The electrical field vector E indicates the direction of the photons' polarization plane. On the right, a Compton scattering event, with a scattering angle (labeled $\mathbf{\Theta}_C$) of 90°. Illustration taken from [20].

Figure 3 below shows a specific simulation example of the theoretical distribution of double events in a CdTe pixel matrix. The generated model demonstrates a Compton scattering event in the central pixel, followed by a photoelectric absorption of the scattered photon in a peripheric pixel. In Figure 3a, the distribution exhibits an oblong shape produced from the simulation of a 100% linearly polarized beam at 200 keV, normal to the detector surface with a polarization angle of 30°. In this case, the main scattering axis distribution is perpendicular to the polarization vector. Figure 3b represents the same simulation, however with an unpolarized incident beam shown without a preferred scattering direction visible on the simulation map.

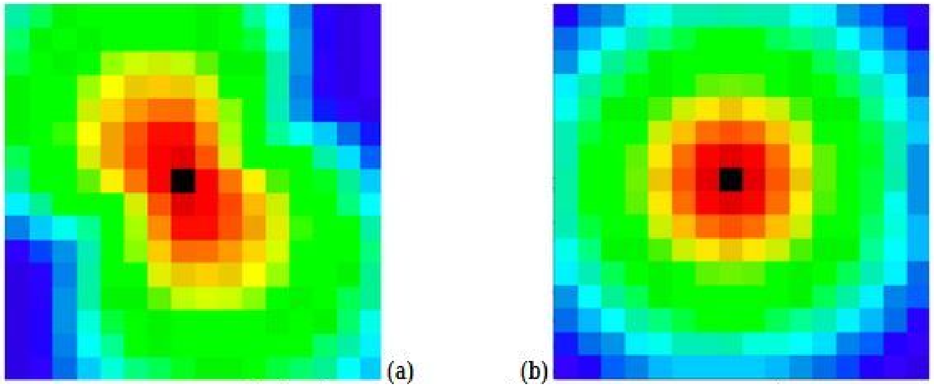

Fig. 3 (a) - 100% linearly polarized beam with an angle of polarization of 30°.
Fig. 3 (b) - Unpolarized photon beam.
Both images represent the numerical simulations of a 200 keV beam, where red indicates high probability and blue indicates lower probability. Images taken from [21].

1.3 Scientific Goals of Balloon Flight Experiment

1.3.1 Scientific Goals

Extensive polarimetric analysis with CdTe prototypes has been conducted, both by simulation and experimentally. A balloon experiment is highly suitable for further analysis of parameters critical to designing a γ-ray polarimeter for space applications. Since celestial-source polarimetric measurements are not likely achievable during a balloon flight due to very low γ-ray flux at balloon altitude combined with detector sensitivity limitations within a balloon payload, measuring the double events' background would be notably useful in determining the expected sensitivity of the instrument's space configuration.

Polarimetric sensitivity has a strong dependence on background noise, therefore measuring the double events produced by background radiation should provide critical information for further polarimeter development. Thus far, data is available exclusively for single events' background. By measuring the double events' background, as well as that of multiple events (photons undergoing more than two interactions in different pixels), and incorporating this data with data for known single events, we would then be able to estimate all possible background components; therefore, obtaining a far more precise background flux will allow for optimizations in future instrument design with respect to minimization of expected space background.

1.3.2 Previous Flight Experience

Our Stratospheric Spectropolarimeter Gamma-X (SSGX) payload is based on the detection capacities of the Compact Array of Cadmium Telluride Micro Spectrometers (CACTμS), [22]. During a twelve-hour balloon flight, launched from Sicily, Italy, in 2002, the CACTμS instrument collected data exclusively for single events' background. We now propose to explore the implementation of coincidence logic for double and multiple events. Double events (two hits within different pixels, the first interaction being a Compton) are essential in determining Compton photons' new direction and therefore the polarization direction.

The CACTμS instrument includes the primary detector housing (CdTe detectors) with associated front-end electronics (voltage supplies, temperature sensors, Charge Sensitive Preamps/CSPs), shown below.

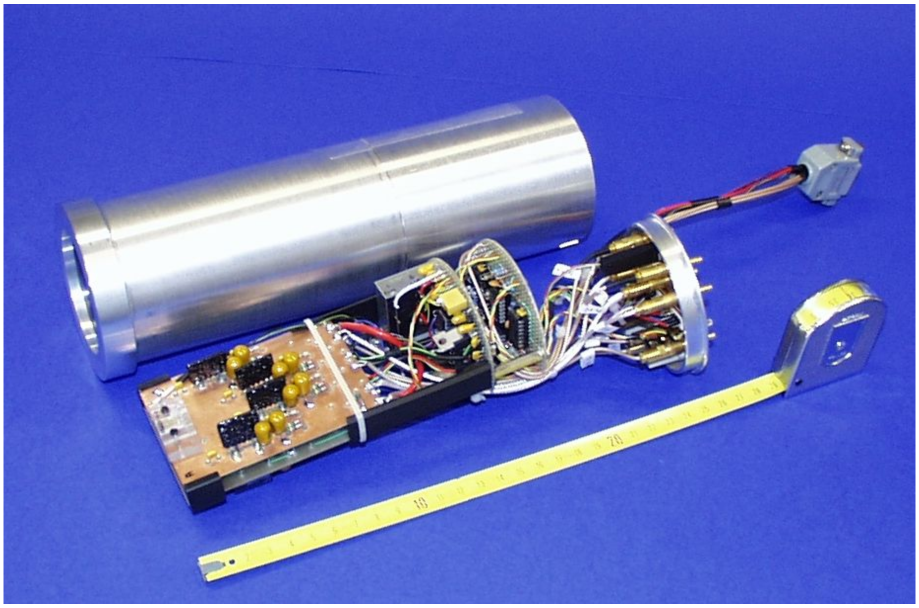

Fig. 4 - CACTμS detecting units housed in a light-tight and airtight container together with the front-end electronics, the voltage supplies, and the housekeeping sensors for remote monitoring. At left, the CdTe sensors containers board including the front-end CSPs; at center, the DC-DC converter and bias filters; at right, the output connectors. (CACTμS collaboration image)

The CACTμS detection unit consists of two CdTe solid-state detector arrays operating at room temperature (see Fig. 10). Each CdTe crystal is divided electrically by a set of four metallic strips deposited on one face, while on the opposite face there is a common electrode connected to ground. The pitch distance between the strip center is 2 mm (1.8 mm wide metallic strip in addition to a 0.2 mm gap). Each strip is a positively biased (nominally +120V) independent electrode on which the charge delivered by an X-ray event is collected and amplified by a conventional Charge Sensitive Preamplifier (CSP). In this way, each CdTe detector is equivalent to four bar-shaped units with a base of 2 mm x 2 mm (orthogonal to the optical axis) and a thickness of 10 mm.

With respect to other former CACTμS' electronics subsystems, our new SSGX payload represents a major upgrading with substantial downsizing in both weight and dimensions of the service electronics. The image below shows the large dimensions of CACTμS' subsystems that included the analog front end electronics (AFEE) box, the Pulse Code Modulation Unit (PCM), the scientific Data Handling System (DHS) with Analogue to Digital Conversion (ADC) and digital control electronics, and the Telecommand/Telemetry unit. These would easily occupy all of the space allotted for the four large payloads as accommodated by HASP. Details are given further below about the current, much smaller integrated electronics systems recently developed at ARC, which will interact with the detector unit inherited from the original CACTμS payload.

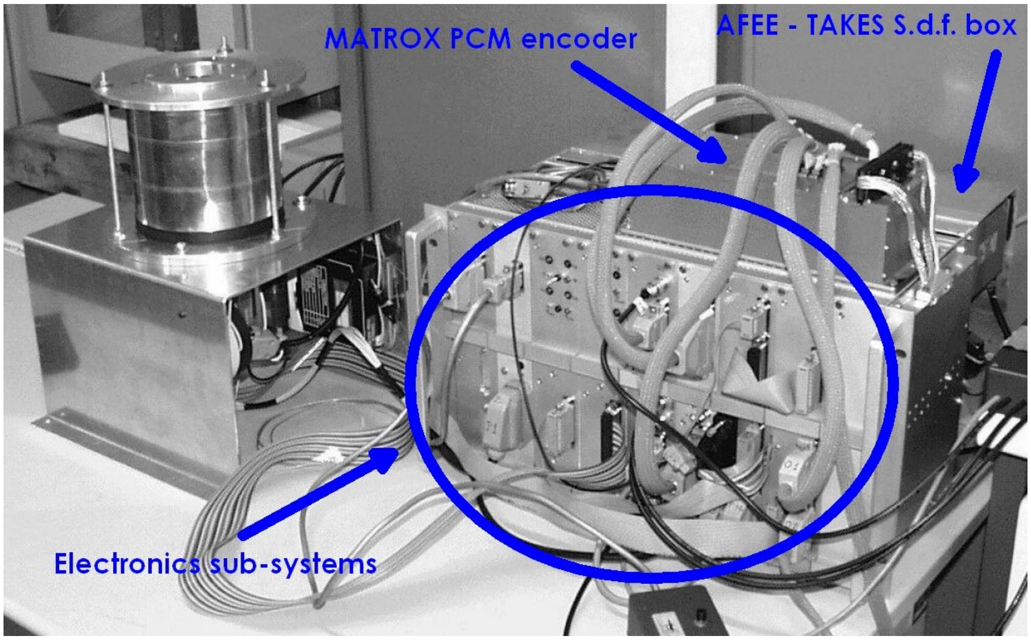

Fig. 5 - Portions of CACTμS electronic subsystems are pictured here. At left, the detecting CdTe units cylinder, which remains with all of the new SSGX payload electronics. The large electronics system indicated by the circle at right has since been replaced by the Data Acquisition/Integrated Storage Interface (DAISI). (CACTμS collaboration image)

In terms of thermal behavior and "housekeeping", all CACTμS systems performed well during the twelve-hour flight; we expect similar results from a longer HASP flight. All voltage supplies, including the two voltages biasing the CdTe detector, were continuously monitored during the flight with data transmission in the Telemetry (TLM) format. During the entire flight, none of the monitored voltages deviated from the nominal value by more than twice the quantization uncertainty (±40 mV), thus confirming the reliable operation of all CACTμS subsystems.

The in-flight monitored temperatures deviated from their values at ground due to the thermal gradients with respect to the external environment. Fig. 6 below shows the temperature range of the payload electronics and CdTe detector recorded during the flight; the temperature of all other CACTμS subsystems demonstrated a trend similar to those shown in Fig. 6.

The detector temperature drift from +28 °C down to approximately -6 °C did not influence the overall detection apparatus, since in-flight automatic gain and offset corrections were continuously performed inside the analog processing electronics.

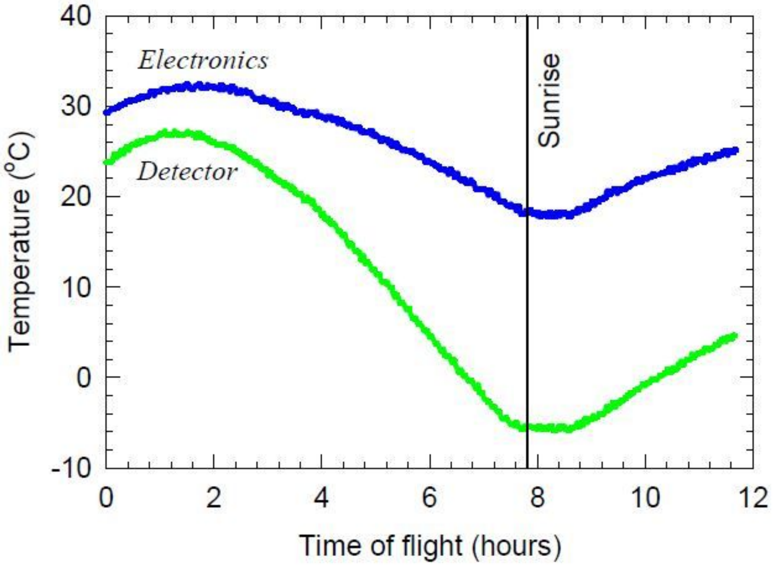

Fig. 6 - The recorded thermal behavior of the CdTe detector and electronics temperature is shown here, expressed as a function of flight time. The balloon was launched at 23:30 local time (Milo, Sicily, Italy), thus flying primarily during cool overnight hours.(CACTμS collaboration graphic)

The entire detector subsystem is contained inside a light-tight aluminum cylinder. Furthermore, all additional subsystems were packed inside a polystyrene box which was then wrapped with Mylar.

Although the HASP flight can exceed durations of 20 hours – thus, for substantially longer than the previous twelve-hour flight of CACTμS – a more recent flight of a CdTe sensor over Svalbard, Norway proved equally thermally successful with polystyrene and Mylar thermal protection.

Despite the favorable results of the previous flight, the new SSGX payload nevertheless applies an active, dedicated thermal protection system as discussed further below.

Finally, we rely on the prior radioisotope ground laboratory energy-channel calibration results of the CACTμS team for in-flight calibration and monitoring of all sensor channel offsets and gains. We will also utilize a "test-in" signal in the CACTμS detector to provide known voltages for real-time calibration. This is necessary to compensate for analog channel gain and offset drift during the flight due to variations in temperature and other environmental parameters such as pressure, humidity, and magnetic field intensity.

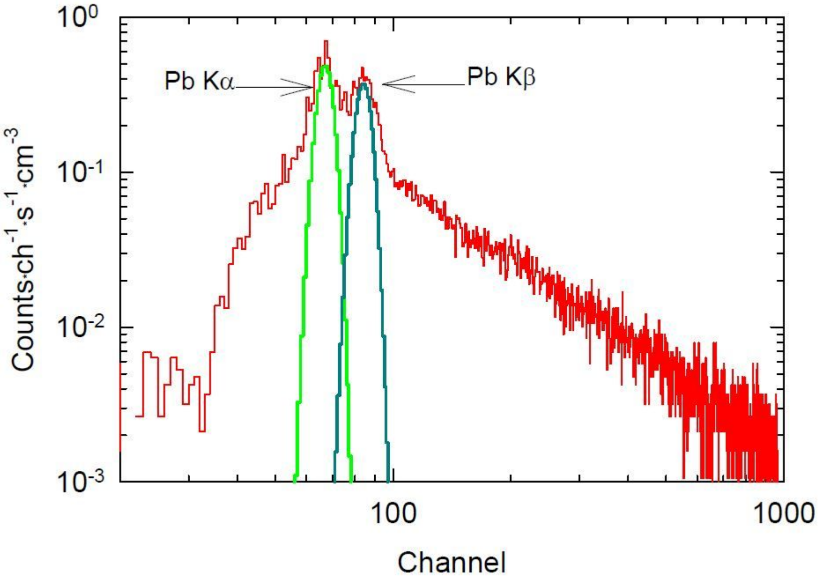

Fig. 7 - This graph shows the energy spectrum detected during CACTμS' flight, including the Pb K-lines generated by the the 2mm thick lead cylinder surrounding the CdTe array. (CACTμS collaboration graphic)

1.4 Payload Systems and Operation

1.4.1 Detection System

Fig. 8 - The CACTμS CdTe detection cylinder and cabling are shown here.

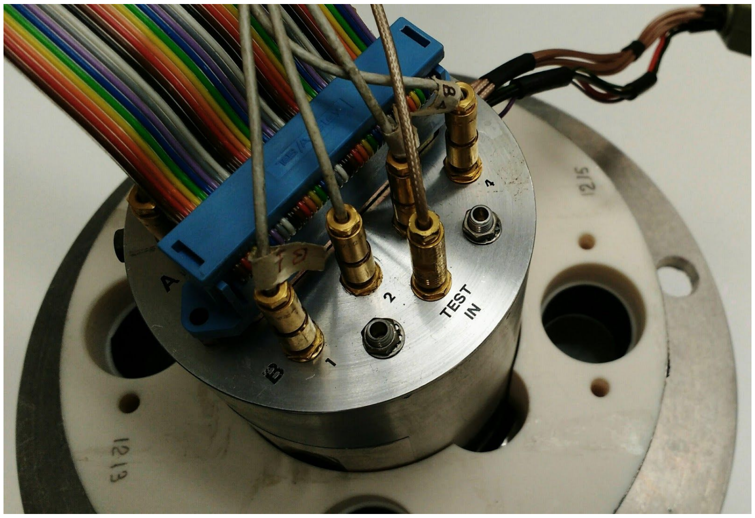

Fig. 9 - A closeup view from the bottom of the detector cylinder, featuring connections.

Cadmium Telluride (CdTe) Detector

The cadmium telluride spectrometers are photovoltaics sensitive to x-ray and γ-ray radiation. When grouped into a pixel array, they can be utilized to determine the intensity, location, and polarization of the measured radiation. The detector consists of two wafers, each split into four strips which independently output an analog voltage dependent on the intensity of the radiation received by the strip. With the wafers stacked and oriented at 90° with respect to each other, the resultant 4x4 pixel grid permits the location of an event to be determined within the detection area. The CdTe detector operates utilizing a 120 V bias, which is generated within the detector cylinder with an EMCO DC-DC converter from a 12 V input.

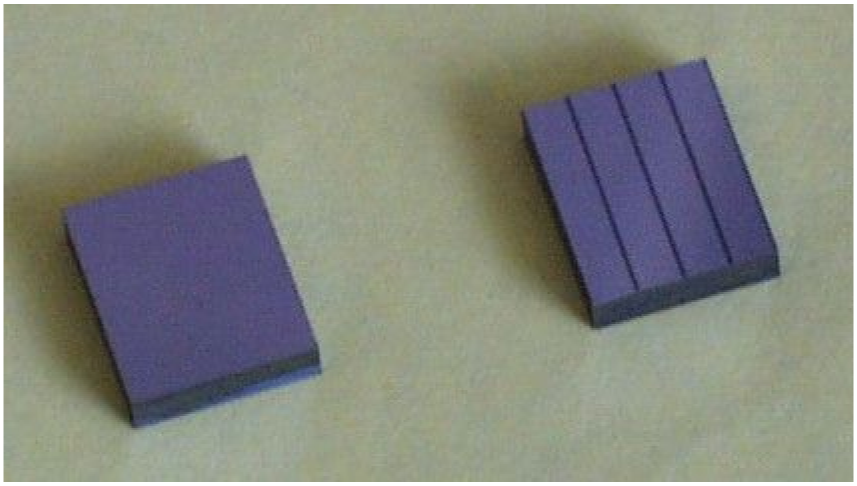

Fig. 10 - The two ACRORAD (10x10x2 mm^3 sensitive volume) CdTe micro-strip units from the photovoltaic detector. The planar cathode surface is shown at left, the multi-strip segmented anode side at right. The detector has a total of eight channels that are currently read by an eight channel analog-to-digital converter (ADC) featuring programmable gain. (CACTμS collaboration image)

1.4.2 Payload Subsystems

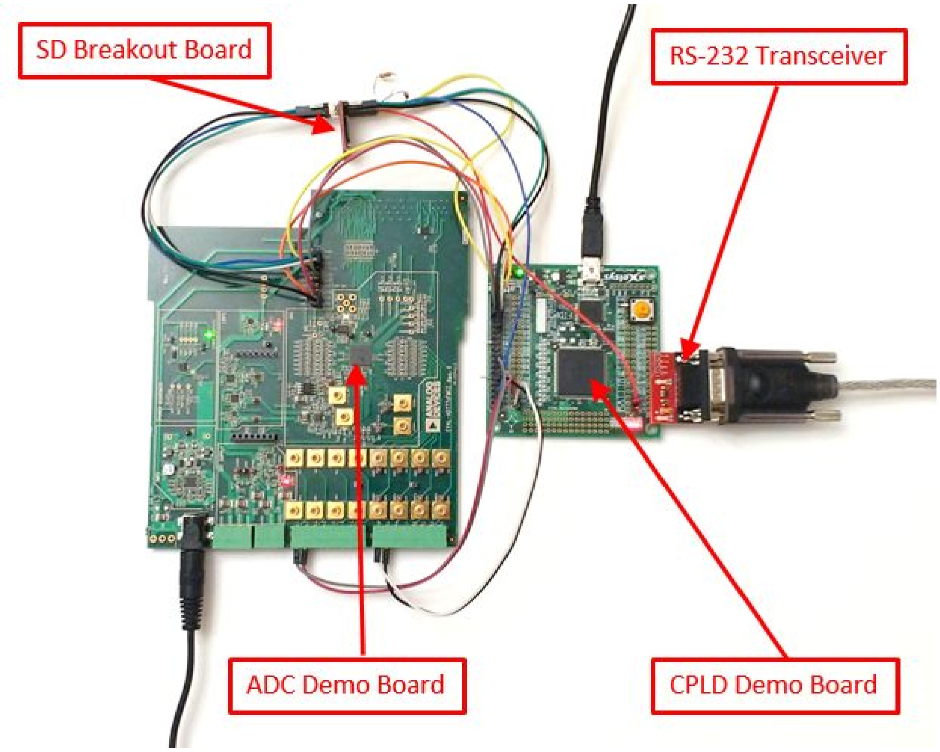

Fig. 11 - The DAISI Prototype is shown here, displaying off-the-shelf demonstration boards from component manufacturers, connected and programmed with early development firmware as a proof of concept for data collection and communication

DAISI (Data Acquisition/Integrated Storage Interface) is an electronics platform developed by the American River College Physics & Astronomy Club, designed to collect sensor data from multiple sources, monitor and regulate system functionality, and record collected data to an SD card. The primary data collected consists of analog voltage levels from the array of eight CdTe strips for the purpose of recording x-ray and γ-ray events. Additional data collected includes system voltage levels, detector and electronics temperatures, and system status such as error states. This data is also saved in real time to an SD card for post-flight evaluation, and instantaneous readings of all data may also be queried utilizing an RS-232 interface. The RS-232 interface is further capable of receiving commands to override and adjust automatic functionality. Finally, through monitoring of the electronics temperature, onboard logic can respond by activating resistive heating elements for purposes of thermal regulation, ensuring that all components remain within appropriate thermal tolerances. A brief description of the major electronic components utilized in the DAISI platform is provided below.

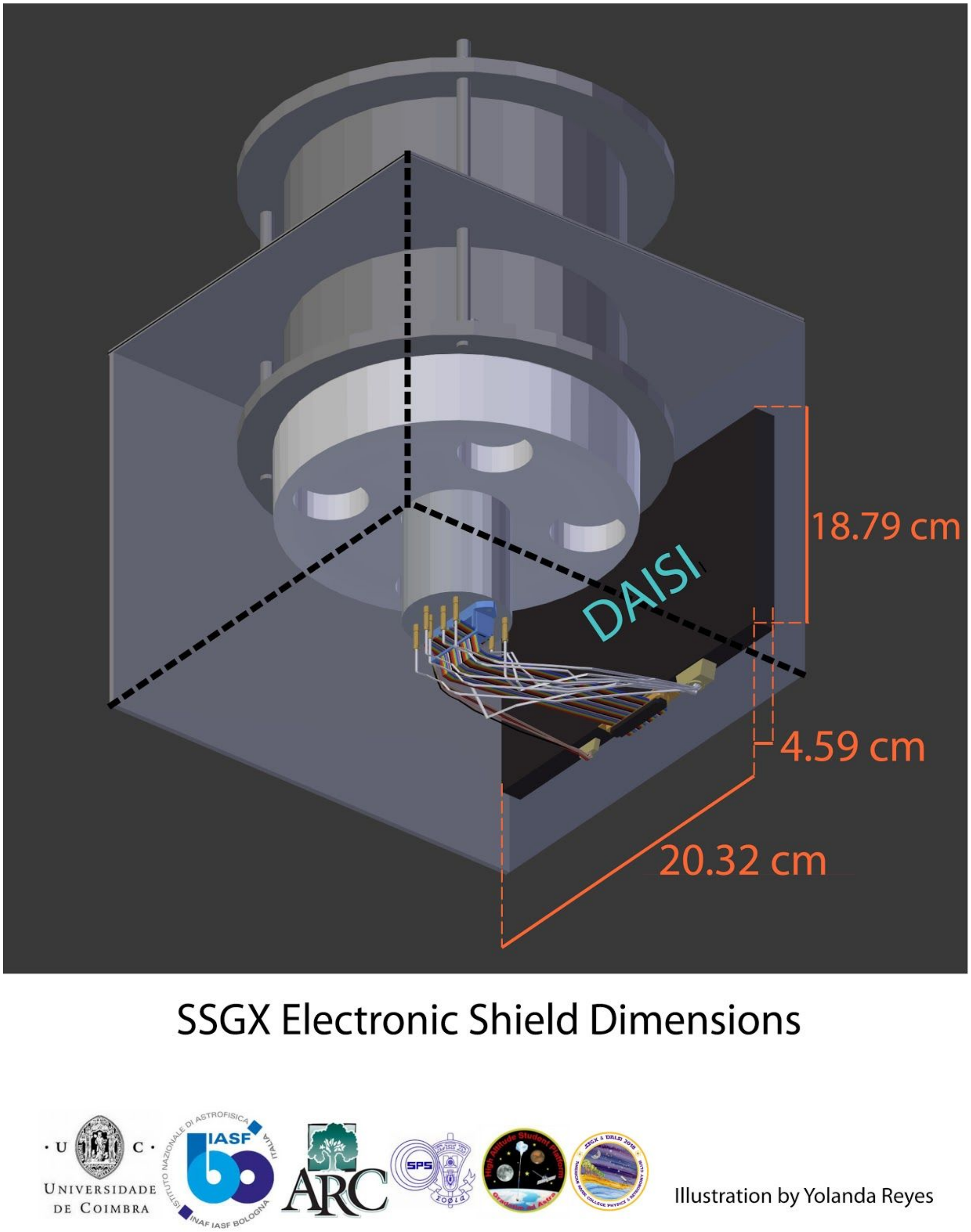

Fig. 12 - The DAISI electronics is housed in an aluminum alloy box shown here. This enclosure provides shielding against RF interference by radio communication transmissions originating from the HASP platform itself, as well as protect against potential electromagnetic interference induced in the electronics by other payloads.

HASP Interface - Voltage Generation and Communication

The HASP interface connects with the cabling of the HASP balloon, providing the main electrical source of a minimum 29 volts and a maximum 2.5 amps. The interface additionally facilitates remote digital communication via RS-232 protocol. Voltage regulators utilize the main voltage supply provided by the HASP interface for generating all local voltage levels required to power all DAISI electronics while simultaneously providing the necessary voltages for the CdTe detector. Many of these regulators may be enabled or disabled by the Complex Programmable Logic Device (CPLD) to manage inrush current at system startup. Regulators may further provide for recovery of error conditions through the power-cycling of individual components during operation. An RS-232 transceiver interfaces with the serial communication port on the HASP balloon for communication with the outside world. It is comprised of a voltage level shifter, which translates the +/- 15 V RS-232 signal voltage from the HASP interface to the 3.3 V range utilized by the CPLD.

Primary Data Collection

The analog-to-digital converter (ADC) is an integrated circuit responsible for the measuring of analog voltage levels from the CdTe detector at a specific point in time, representing that value as a signed 24-bit digital number. Each sample also includes an 8-bit cyclic redundancy check (CRC) value which permits the validation of each sample. The ADC additionally includes independent programmable gain amplifiers (PGA), allowing for the adjustment of the signal gain for each analog voltage channel. The ADC is capable of sampling at a maximum rate of 16 000 samples/second with included signal-shaping filters based on the selected sampling rate. Additional signal offset and gain can be applied in real time through on-chip diagnostic functions and the detector test interface, allowing for signal corrections over time in response to changes due to variations in environmental conditions.

Data Processing

A CPLD is a general-purpose digital circuit made up of numerous configurable blocks that can be programmed to perform multiple custom operations simultaneously. For this project, the CPLD is responsible for managing the system startup, collecting the regular readings of digital ADC output values, collecting detector and electronics temperatures, sampling all regulator voltage levels, and packaging these readings into a standard format that is written to the onboard SD card storage device. The CPLD also utilizes temperature data from the electronics to determine when heating elements should be activated in order to ensure that all components remain within the temperature tolerance necessary for operation. The CPLD monitors the RS-232 interface for incoming data and responds to commands from the HASP communication interface.

Data Storage

This is an SD card interface which acts as the permanent data storage device for all collected data written by the CPLD. This data includes the CdTe sensor analog voltages, detector and electronics temperature data, regulator voltage levels, and system status. Data is written to the SD card in 512 byte data blocks at a rate of 0.386 MB/s. Industrial temperature grade SD cards hardened for x-ray exposure are utilized for this system, with two SD cards being utilized simultaneously for data redundancy. The data stored in the SD card is retrieved after the flight and examined utilizing PC-side software for scientific analysis.

1.4.3 Firmware Design

CPLD: Overview

The CPLD is the main processing unit within the DAISI electronics platform; it is responsible for simultaneously acquiring and saving data, determining system performance, and responding to changes in device status. A CPLD is a general-purpose digital circuit made up of numerous configurable blocks that can be programmed to perform many custom operations concurrently. Utilizing a CPLD affords multiple benefits absent from microprocessor options, including low power operation, high clock rates, and truly simultaneous processing capabilities.

The CPLD logic is coded using the Verilog programming language, which has been divided into functional modules as pictured below. For this project, the CPLD is responsible for managing the system startup, collecting the regular readings of digital ADC output values, collecting detector and electronics temperatures, sampling all regulator voltage levels, and packaging these readings into a standard format that is written to the onboard SD card storage device.

The CPLD also utilizes temperature data from the electronics to determine when heating elements should be activated in order to ensure that all components remain within the temperature tolerance necessary for operation. The CPLD monitors the RS-232 interface for incoming data and responds to commands from the HASP communication interface.

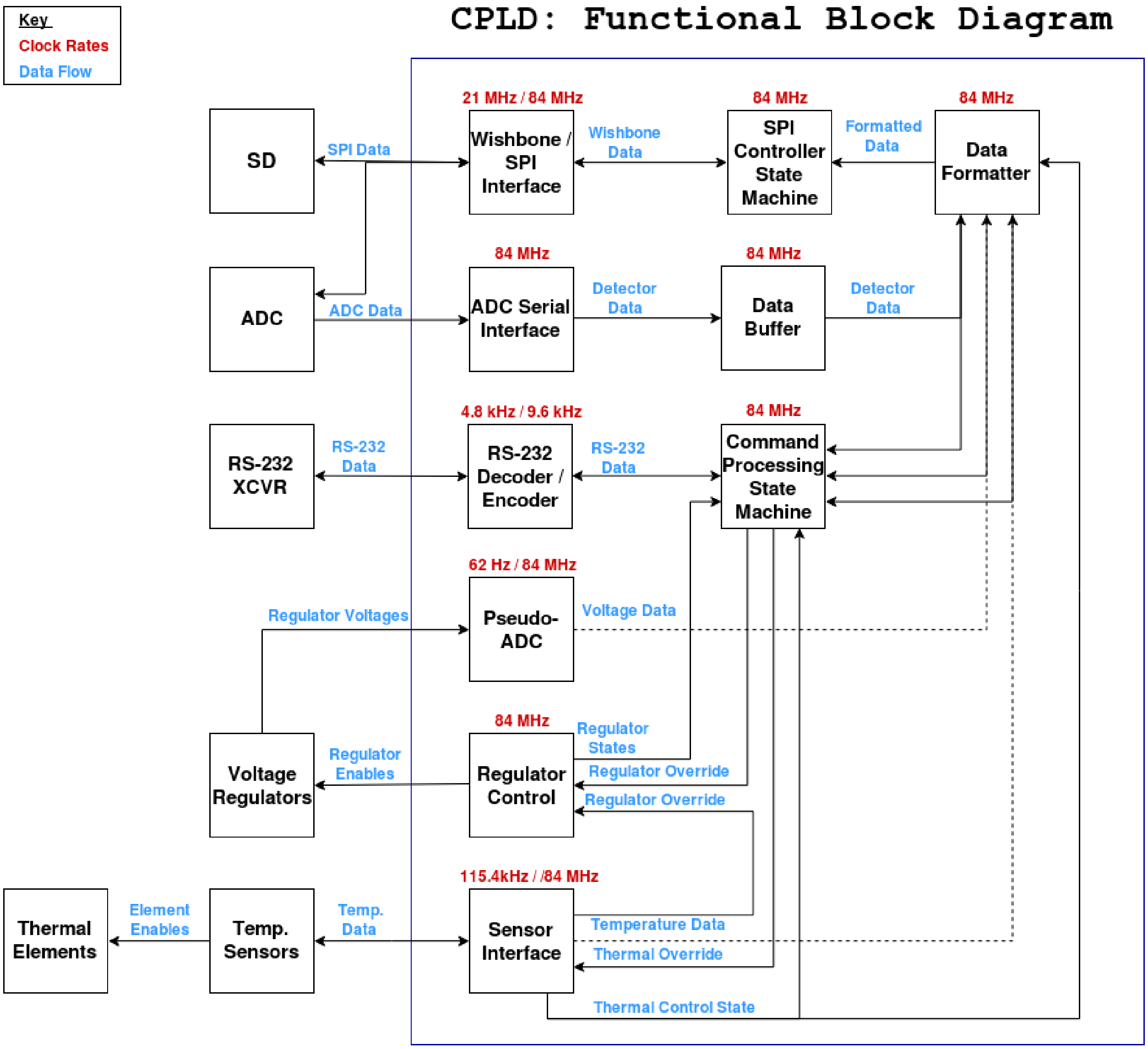

Fig. 13 - This block diagram details the internal CPLD modules which have been coded to simultaneously process incoming information and distribute these data between modules coherently.

1.4.4 Thermal Control

Temperature Sensors

These sensors are responsible for taking measurements of local temperature for both the DAISI electronics and the CdTe detector cylinder. There are four temperature sensors integrated into the DAISI electronics. Each temperature sensor within the DAISI electronics operates over a range of -55 °C to +125 °C, with 14-bit resolution and includes programmable output pins. These outputs will be utilized for active temperature regulation by toggling switches connected to resistors used for heat dissipation.

Heating Elements
Thermal regulation of onboard electronics is achieved by a set of resistive heating elements which can be actively enabled or disabled by the CPLD through the temperature sensor local to the element. On the final custom Printed Circuit Board (PCB) there will be four of these regulation circuits, with one placed at each corner of the PCB. The resistive heating elements will conduct thermal energy through planes of copper within the PCB, directly heating the electronic components. When active, each resistive element will contribute a +27 ºC differential to ambient temperature through power dissipation of 6W. Together, with the heat dissipation from voltage regulators, the active heating elements will behave like a thermostat by switching on the heating elements when the temperature drops below -20 ºC. This maintains consistency of temperature in the electronics during operation which is well above the minimum absolute temperature threshold of the electronic devices.

1.4.5 Anticipated Software Development

Aggregate Software for Technical Execution and Retrieval (ASTER): Overview
ASTER is a user interface programmed in Java by the American River College Physics & Astronomy Club for the purpose of interacting with DAISI in order to translate the collected data into its graphical representation. The software will communicate to the SSGX module using DAISI's RS-232 serial interface through the HASP platform by sending commands to and receive status updates back from the SSGX payload. ASTER will also operate as a front-end software for controlling the SSGX functions as well as present live data transmitted from the module during the flight.

Moreover, during development ASTER will be used to calculate calibration corrections to compensate for any anomalous data. The program uses data extracted from the SD card to generate plots in order to graph energy spectra, single/double events and a visualize the pixel map. All extracted data may also be saved for later viewing in a Comma-Separated Values (CSV) file. Furthermore, ASTER will provide a zoomed-in, windowed display capable of scrolling the graph along a timeline in order to observe specific sections of data. ASTER is capable of extracting and utilizing data from all eight analog channels. When prompted, the program will convert incoming hexadecimal values to voltages and display a scatter plot of the incidental voltages.

II. Team Structure & Management

In June 2014, the ARC Physics & Astronomy Club successfully launched and retrieved a small three Kg payload balloon in California's Mojave Desert. With a flight duration of approximately two hours, the balloon was equipped with commercial GPS, flight cameras, and an aerogel chamber for microbial capture. Components were controlled via Raspberry Pi microcomputer utilizing Python code developed by the group.

Aiming to develop a praxis of balloon flight at American River College, in 2014-2015 we learned about HASP and subsequently established a collaboration with our experienced senior partners in Italy and Portugal.

The current student-based team consists primarily of S.T.E.M. undergraduates who have greatly expanded the work from previous years and has been meeting for several hours each week since March of this year to advance the interests of this project. Working individually and in groups, students have been developing skills in firmware and logic design, software design and development, schematic design, technical illustration, simulation development, and hardware assembly.

Table 1: Project Contributors

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*** indicates flight control team**

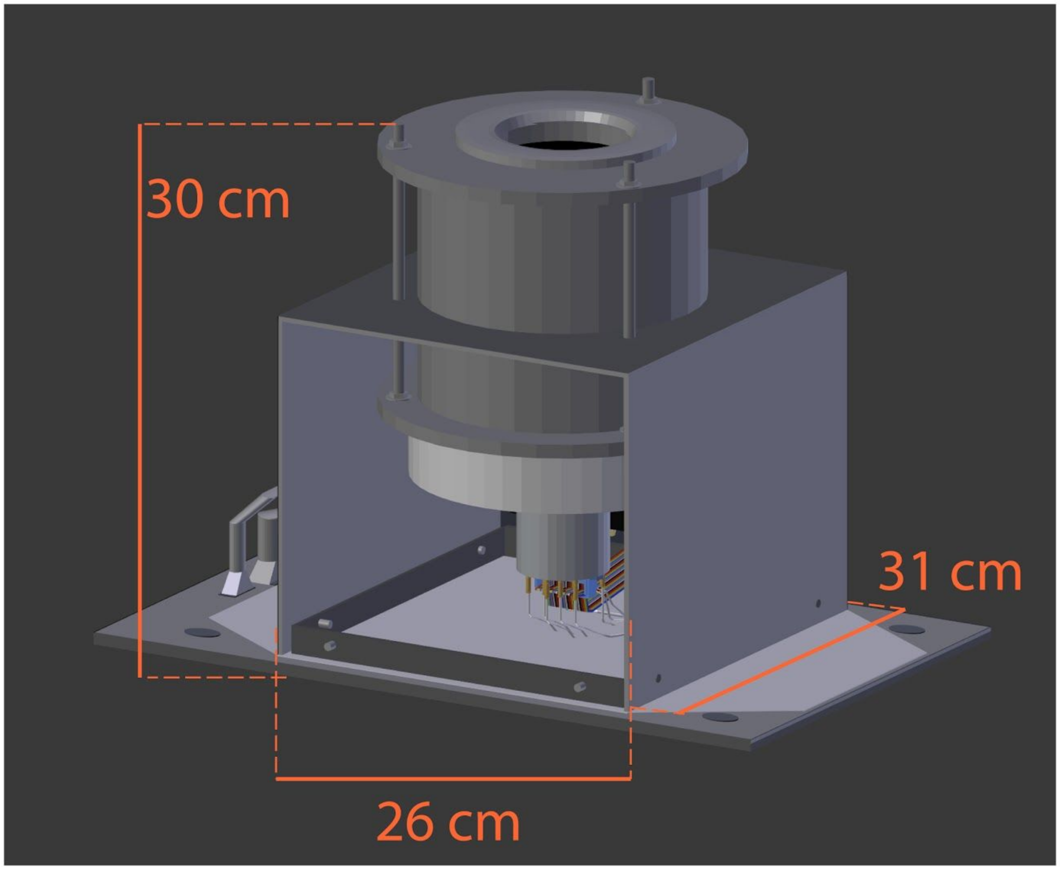
Table 2: Anticipated HASP 2017-2018 Development Timeline

Date	**Development Goal**
December 2017	● Complete and submit HASP application ● Evaluate and refine detector signal shaping ● Evaluate prototype performance over long sampling times ● Validate and finalize all circuit schematics ● Complete initial PC software control interface
January 2018	● Complete PCB layout and submit for manufacturing ● Complete PC software windowed scatter plots for all sensor types
February 2018	● Assemble and validate all PCB subsections

	● Complete electronics noise minimization ● Complete PC software visualization for all desired plot types ● Acquire all required materials for main housing assembly
March 2018	● Complete initial pressure and temperature testing ● Complete all detector sensor readout calibrations using high-energy photon emissions ● Complete PC software calibration interface ● Complete mounting bracket installation onto mounting plate
April 2018	● Complete and validate automatic in-flight calibration adjustment routines based on software calibration results ● Complete assembly of main SSGX housing ● Submit preliminary PSIP document
May 2018	● Finalize documentation of SSGX dimensions and detailed mounting plan for submission ● Finalize documentation of DAISI electrical properties ● Submit monthly status report ● Attend HASP teleconference
June 2018	● Prepare for payload integration ● Submit final PSIP document ● Submit monthly status report ● Attend HASP teleconference
July 2018	● Complete payload integration at CSBF ● Submit final FLOP document ● Submit monthly status report ● Attend HASP teleconference
September 2018	● HASP flight preparation ● Target flight ready ● Target launch date and flight operations ● Payload recovery and shipping ● Begin post-flight data analysis ● Submit monthly status report ● Attend HASP teleconference
August 2018	● Submit final monthly status report ● Attend HASP teleconference ● Continue post-flight data analysis
October - November 2018	● Perform post-flight data analysis ● Complete data analysis required for HASP science report ● Complete flight and science report
December 2018	● Submit final flight / science report

III. Payload Interface

3.1 Payload Dimensions



SSGX Payload Dimensions

Illustration by Yolanda Reyes

Fig. 14 - SSGX payload dimensions are shown here.

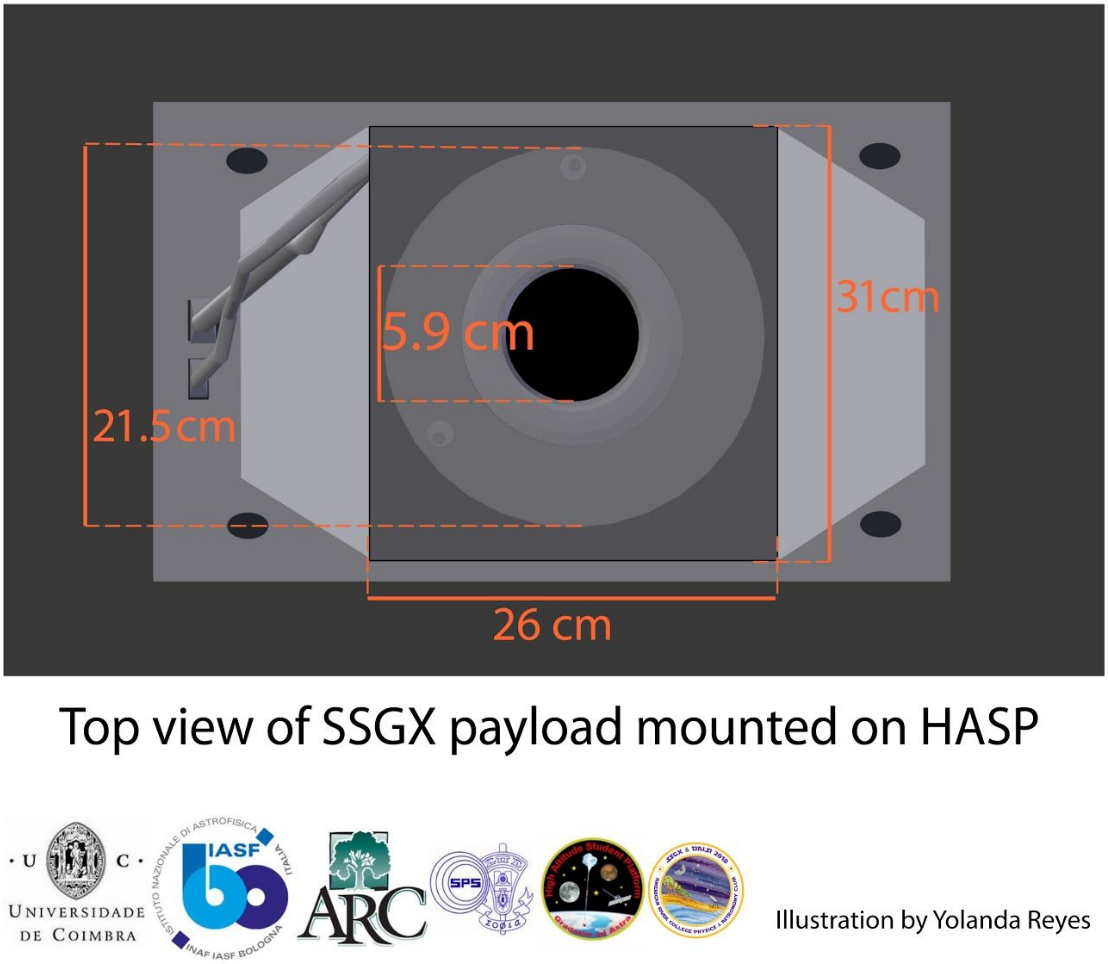


Fig. 15 - Top view of SSGX payload mounted on the HASP platform.

3.2 Weight Distribution

Table 3: Weight Budget

Component	**Mass (kg)**
Detector Cylinder with Cables	5.90
Payload Housing	3.50
DAISI Electronics	0.15
Electronics Shield	0.44

Total (kg)	**9.99**

3.3 Mounting Plan

Using Weld-on 2007 solvent cement for rigid and foamed vinyl, we will cement and mount a 4.57 cm tall PVC bracket to the provided 0.635 cm thick HASP payload plate. We will use eight 1.9 cm 8-32 flathead screws to attach the main payload housing, including the CdTe detector, to the cemented PVC bracket. These screws will be placed 2.54 cm away from adjacent seams, and 1.27 cm above the HASP payload plate. SSGX may be mounted on any of the large payload positions, therefore we are not requesting a specific location on the platform.

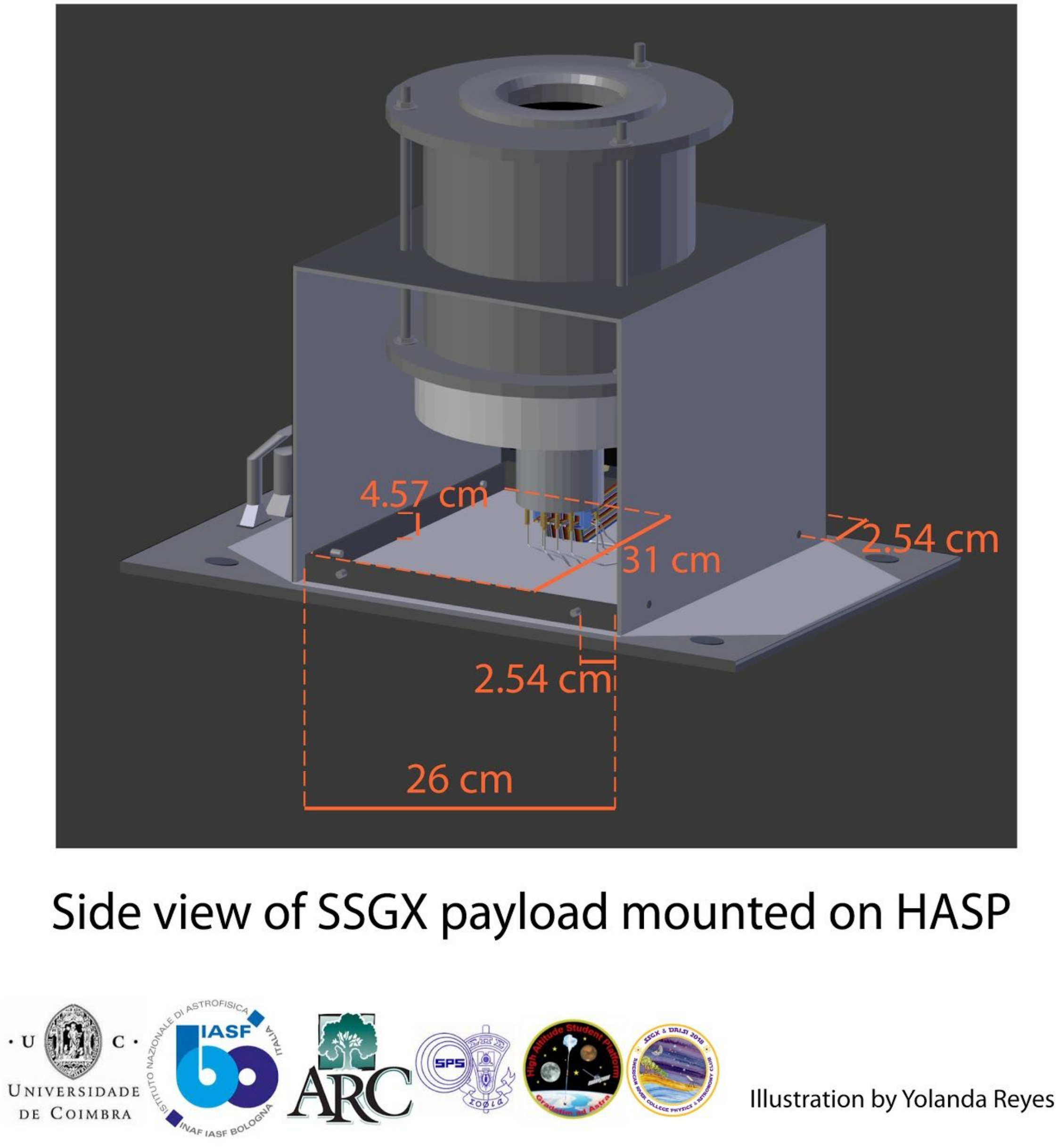
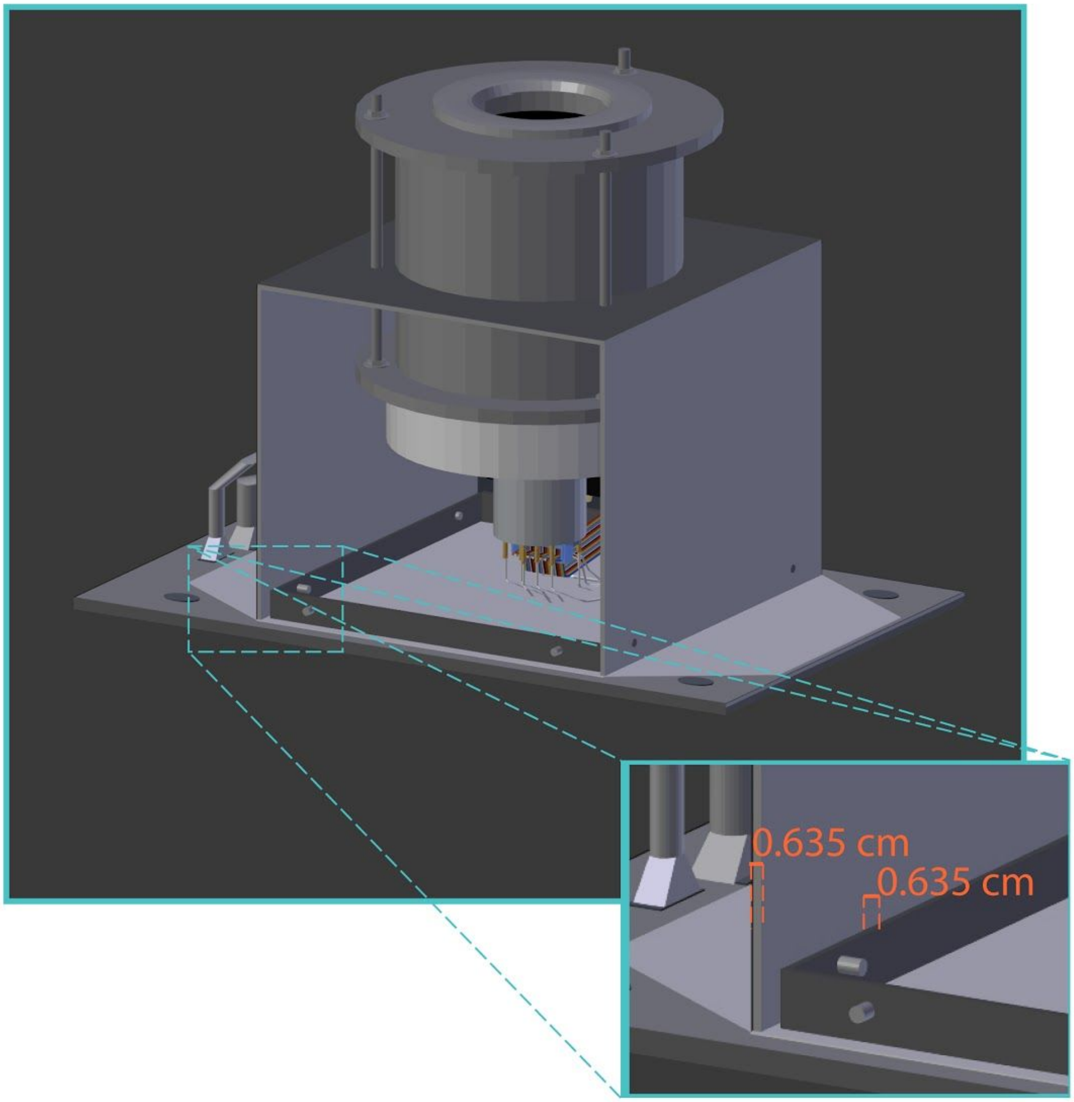


Illustration by Yolanda Reyes

Fig. 16 - Side view of SSGX payload, featuring mounting dimensions



Close up of SSGX mounting bracket on HASP

Illustration by Yolanda Reyes

Fig. 17 - Side view of SSGX payload, detailing the mounting bracket on the HASP platform.

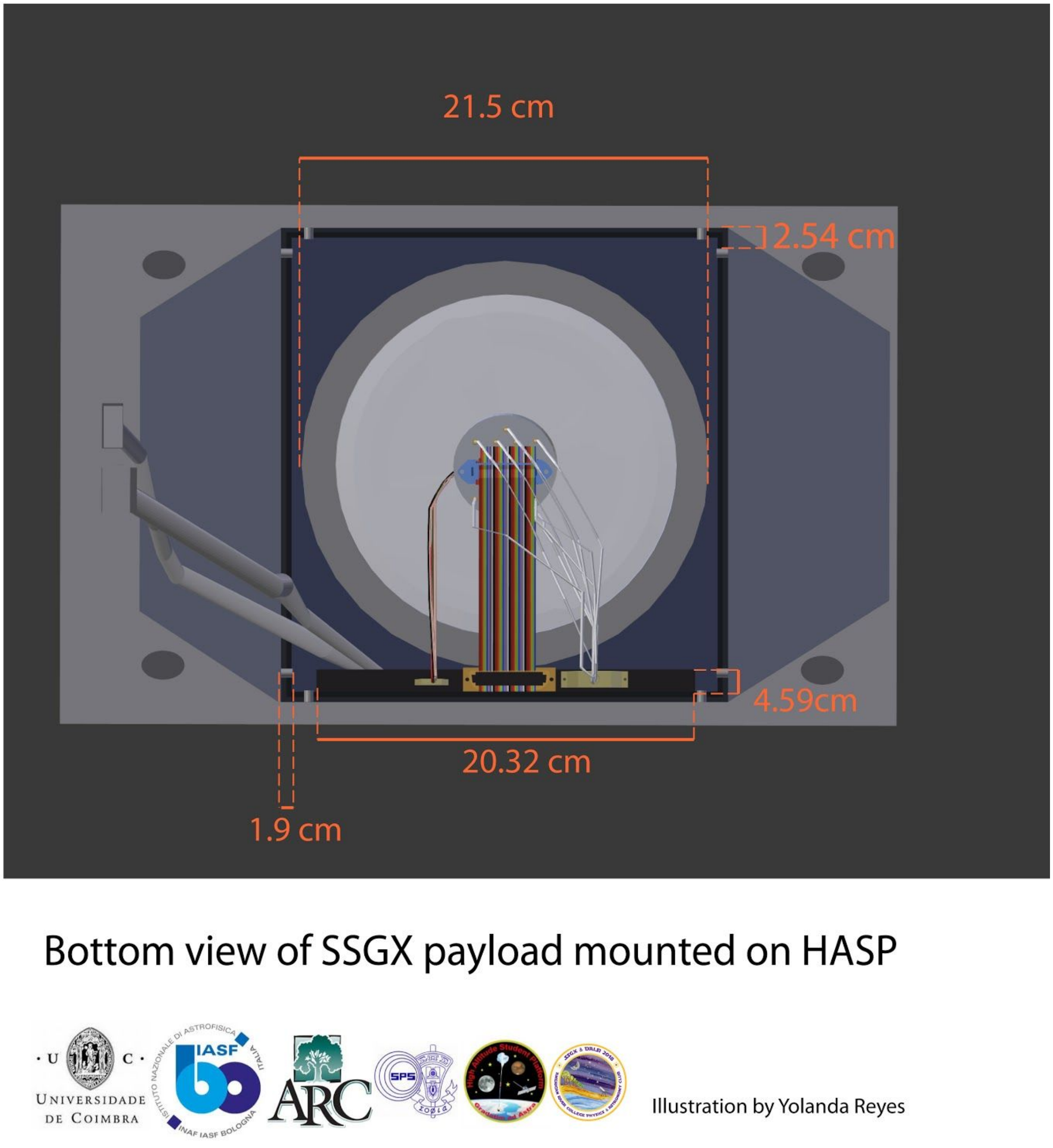


Fig. 18 - Bottom view of SSGX payload mounted on the HASP platform, with the HASP mounting plate made transparent to indicate placement.

EDAC and DB9 connectors from the HASP mounting plate provide pigtail wires for electrical access. The DAISI electronics includes a 5-pin wire terminal header to connect to the pigtail wires from the mounting plate. The table below indicates which connections are utilized by this project.

Table 4: Platform Connections Pin-Out

Header Pin	**Label**	**HASP Pin**
1	30 V Power	A, B, C, D (EDAC)
2	Power Ground	W, T, U, X (EDAC)
3	RS-232 Receive	2 (DB-9)
4	RS-232 Transmit	3 (DB-9)
5	RS-232 Ground	5 (DB-9)

3.4 Electrical Distribution

Voltage Regulators

These components utilize a main voltage supply of 29-33 V from the HASP interface to generate all local voltage levels required to power the DAISI electronics, in addition to providing the necessary voltages for the CdTe detector. Many of these regulators may be enabled or disabled by the regulator control module to manage inrush current at system startup through the staggered powerup of individual circuits, and/or to provide for recovery of error conditions through the power-cycling of individual components during operation. A CPLD module determines when the external voltage regulators are turned on or off. At startup, it will stagger the initiation of each regulator to limit the inrush current when DAISI is first powered. After startup, individual regulators may be enabled or disabled in response to events, such as for the need to power-cycle a device in the event of a communication failure, or in response to commands received by the command processor.

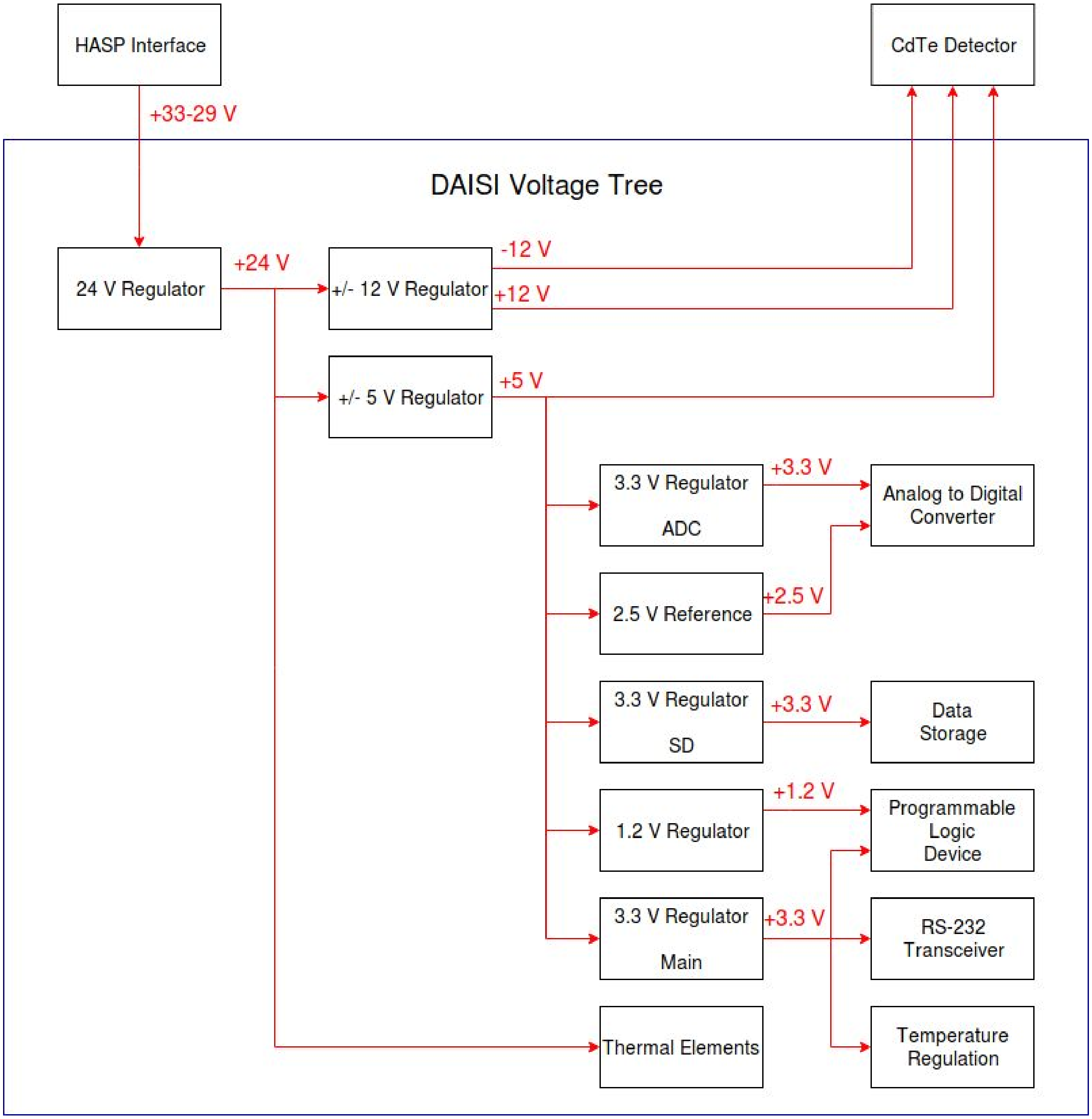


Fig. 19 - Voltage distribution tree indicating which voltage regulators are used to supply power to individual components.

Voltage Monitoring

The voltage output from each onboard regulator is passed through a resistor-divider circuit and used to charge a capacitor connected to a CPLD input/output (IO) line. The capacitor charge time is used by a pseudo-ADC module coded within the CPLD to determine the regulator output voltage levels while the device is operating. This element functions as a low-precision ADC implemented in Verilog and is used to verify the voltage levels output by the various voltage regulators throughout DAISI without the need to provide additional measurement components. The CPLD obtains a digital voltage reading by driving an IO line low in order to discharge the external capacitor, then switches the IO line to a high-impedance state and increments a counter until the voltage on the IO line reaches the threshold necessary for the line to be read as “high.” A greater voltage will require less time to reach this threshold value, allowing the voltage level to be determined. This process is continuously repeated and the results are averaged to produce a final reading at the desired rate.

Component Current Requirements

The HASP platform provides a maximum 2.5 amps to power payload electronics. Table 5 below breaks down the expected current draw from the major components of the system and demonstrates how the SSGX system will remain below the maximum current permitted.

Table 5: Current Consumption

Component	Max Used (mA)
Detector	~200
CPLD	14.35
ADC	47.65
SD x 2	200
RS-232 Transceiver	10
Temp Sensor x 4	1.6
Thermal Element x 4	1000

Total (mA)	**1474**

3.5 Communication Plan

RS-232 Command Processing

Data is received and transmitted through the transceiver, assuming a start and stop bit - without flow control - at a rate of 4800 baud. Within the CPLD, an encoder/decoder module receives the serial data from the RS-232 transceiver in the RS-232 protocol format and makes it accessible as a series of ASCII bytes to a command processing module. Oversampling the incoming data at a rate of 4x to detect bit transitions accounts for possible clock speed differences between DAISI and the HASP platform. The command processor accumulates incoming ASCII bytes, detecting valid combinations which represent commands terminated with a newline character, and parses out variable data within the commands. The command processor also generates response strings after receiving a valid command, passing this string back to the encoder/decoder module for transmission. The command processor is used to check system status, such as current detector ADC readings, regulator voltages, or detected errors. As such, instantaneous data from most modules is provided to the command processor, such that this data may be queried as needed by a user.

Maximum Communication Rate

The ASTER control and monitoring software will poll the system status once every five seconds during the flight, providing a regular system status overview for monitoring. The maximum ASCII bytes transferred per update is 300, including both the command strings and response strings. This allows for an update on the instantaneous detector analog voltages, single and double event counts, system regulator voltages, temperature sensor readings, and the occurrence of any error states without approaching the maximum data throughput allotted by the 4800 baud connection. The team may occasionally send command strings in response to system conditions as well, with each command using a maximum of 12 ASCII bytes for the command and response.

Table 6: DAISI RS-232 Command List

Current Detector Analog Channel Voltage Readings		
Direction	**ASCII String Format**	**Description**
Input	detch<channel number>	Detector channels 1-8 are valid
Output	XXXXXXXX	8 character hex representation of 32-bit ADC sample data for the corresponding analog channel from the detector

Total Detector Single Events Count		
Direction	**ASCII String Format**	**Description**
Input	sevents	
Output	XXXXXXXX	8 character hex representation of 32-bit counter value for detected single events

Total Detector Double Events Count		
Direction	**ASCII String Format**	**Description**
Input	devents	
Output	XXXXXXXX	8 character hex representation of 32-bit counter value for detected double events

Current Regulator Voltage Readings		
Direction	**ASCII String Format**	**Description**
Input	regch<channel number>	Regulators 1-8 are valid
Output	XXXX	4 character hex representation of 14-bit ADC sample data for the corresponding analog channel from the detector

Current Temperature Readings		
Direction	**ASCII String Format**	**Description**
Input	tempch<channel number>	Channels 1-4 are valid
Output	XXXX	4 character hex representation of 14-bit ADC sample data for the corresponding analog channel from the detector

Device Error Conditions		
Direction	**ASCII String Format**	**Description**
Input	errors<device>	system/adc/sd are valid devices
Output	XXXX	4 character hex representation of 16-bit error count value for the corresponding device

Regulator Enable/Disable Controls		
Direction	**ASCII String Format**	**Description**
Input	reg<status><regulator number>	Status set to “En” for regulator enable or “Dis” for regulator disable Regulators 1-8 are valid
Output	<status><regulator number>	Status set to “En” for regulator enable or “Dis” for regulator disable Regulators 1-8 are valid

<table>
<tr><th colspan="3">Thermal Regulation Auto/Enable/Disable Controls</th></tr>
<tr><th>Direction</th><th>ASCII String Format</th><th>Description</th></tr>
<tr><td>Input</td><td>therm<status><element number></td><td>Status set to “En” for element enable, or “Dis” for element disable, or “Auto” for normal firmware control
Regulators 1-8 are valid</td></tr>
<tr><td>Output</td><td><status><element number></td><td>Status set to “En” for element enable, or “Dis” for element disable, or “Auto” for normal firmware control
Regulators 1-8 are valid</td></tr>
</table>

<table>
<tr><th colspan="3">Start/Stop ADC Sampling</th></tr>
<tr><th>Direction</th><th>ASCII String Format</th><th>Description</th></tr>
<tr><td>Input</td><td>adc<start/stop></td><td>Status of “start” begins the ADC sampling process, while “stop” ends ADC sampling</td></tr>
<tr><td>Output</td><td><start/stop></td><td>Start/Stop status confirmation</td></tr>
</table>

<table>
<tr><th colspan="3">Reset System</th></tr>
<tr><th>Direction</th><th>ASCII String Format</th><th>Description</th></tr>
<tr><td>Input</td><td>reset</td><td>System immediately initiates the rebooting sequence, placing all components back to the default operational state</td></tr>
<tr><td>Output</td><td></td><td>No output</td></tr>
</table>

IV. Preliminary Drawings

4.1 Payload and Platform Mounting

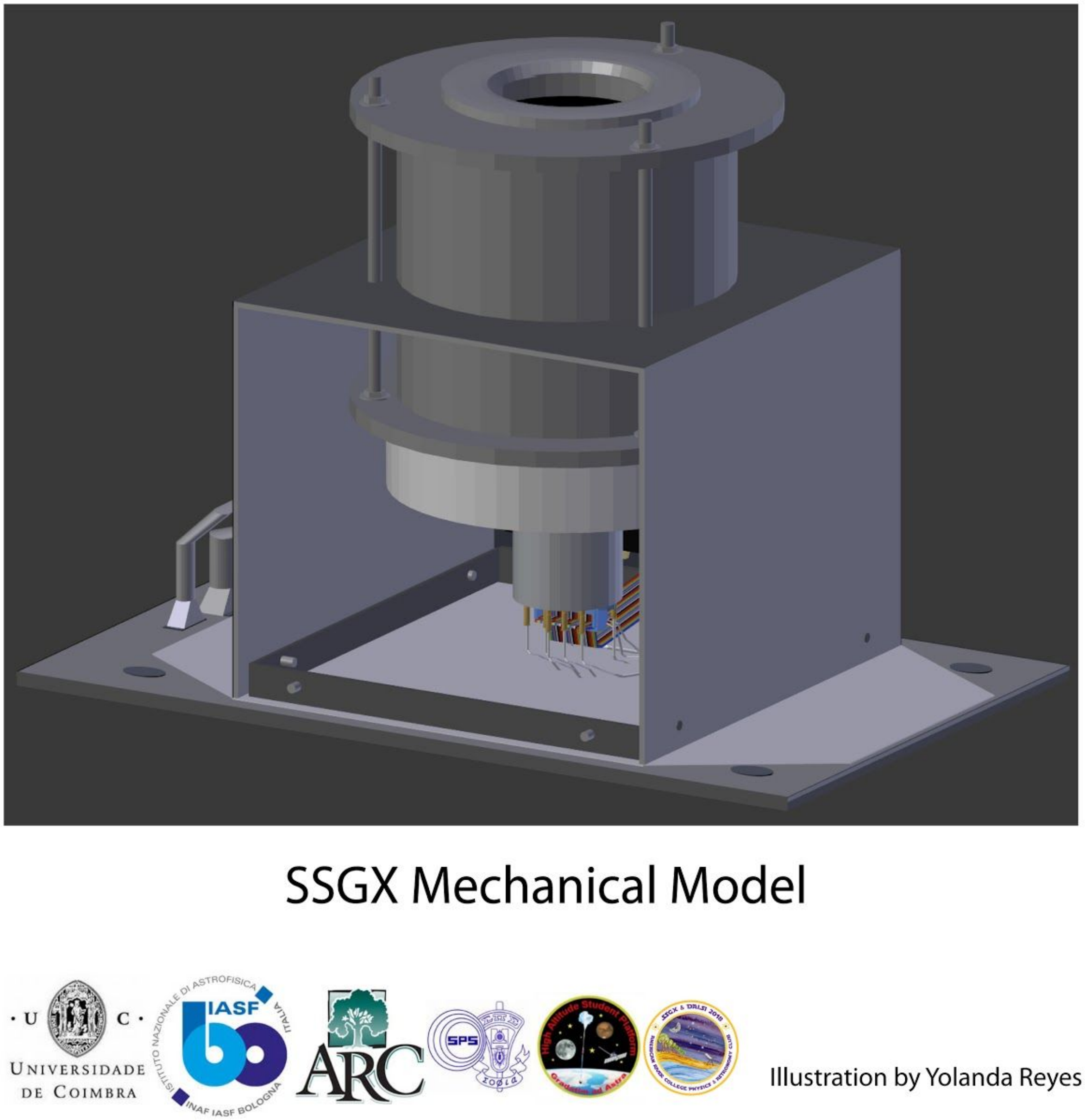


Fig. 20 - The SSGX mechanical model is shown here.

4.2 Power Circuit Diagrams

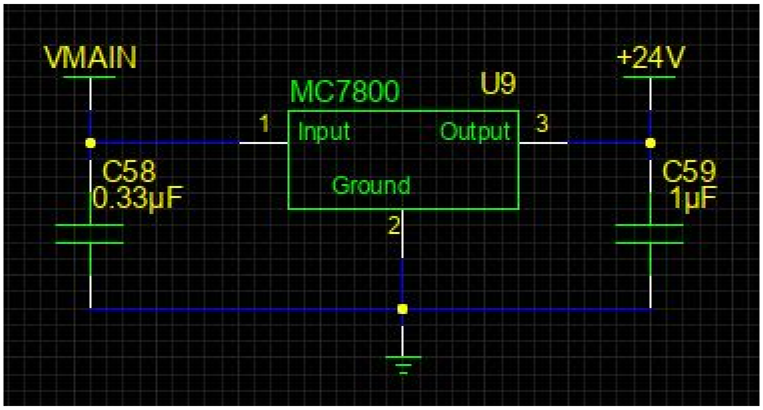


Fig. 21 - Schematic diagram for regulator +24 V down from +33 V to +29 V provided by the HASP platform.

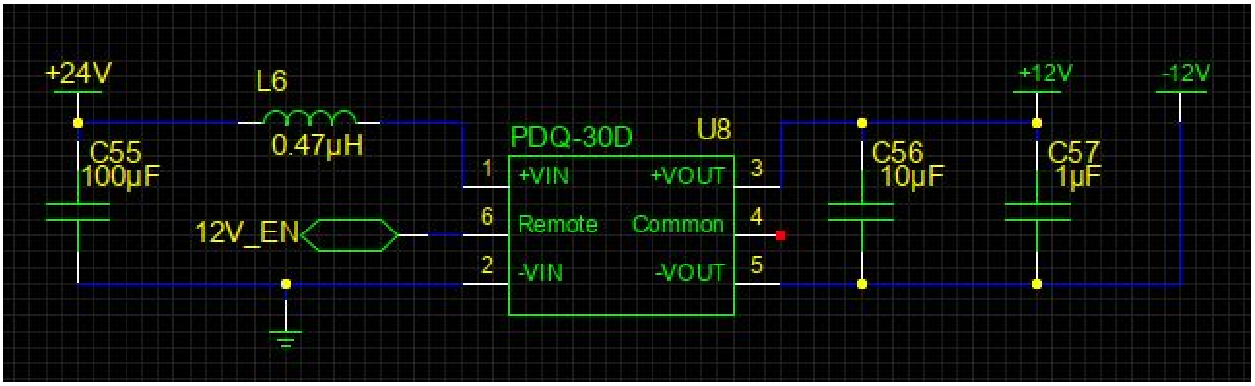


Fig. 22 - Schematic diagram for regulator, +/- 12 V for CdTe detector.

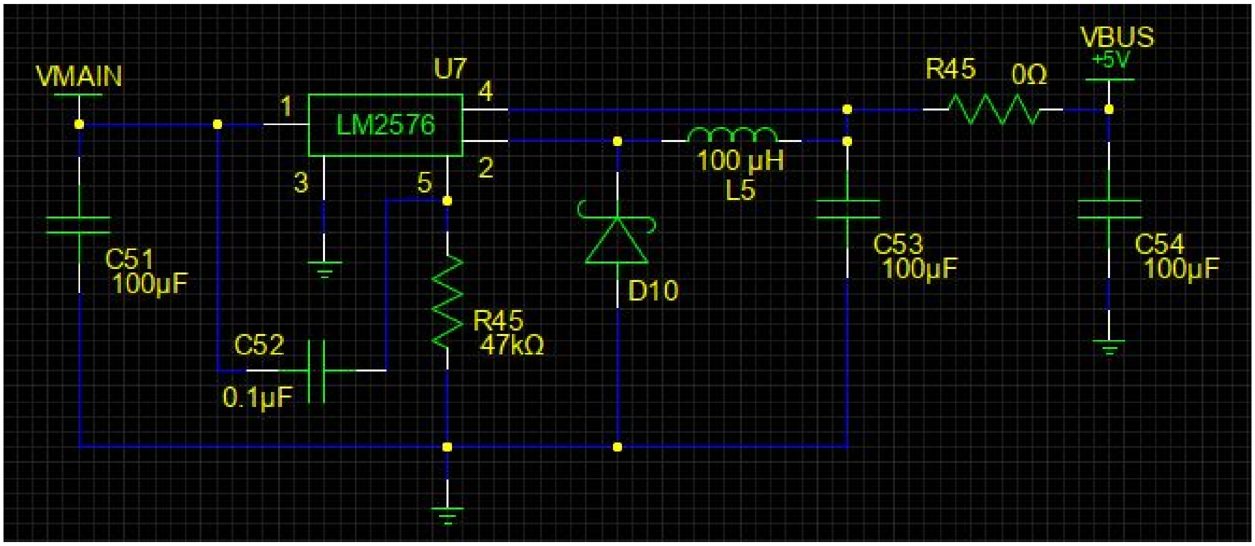


Fig. 23 - Schematic diagram for regulator, +5 V Main.

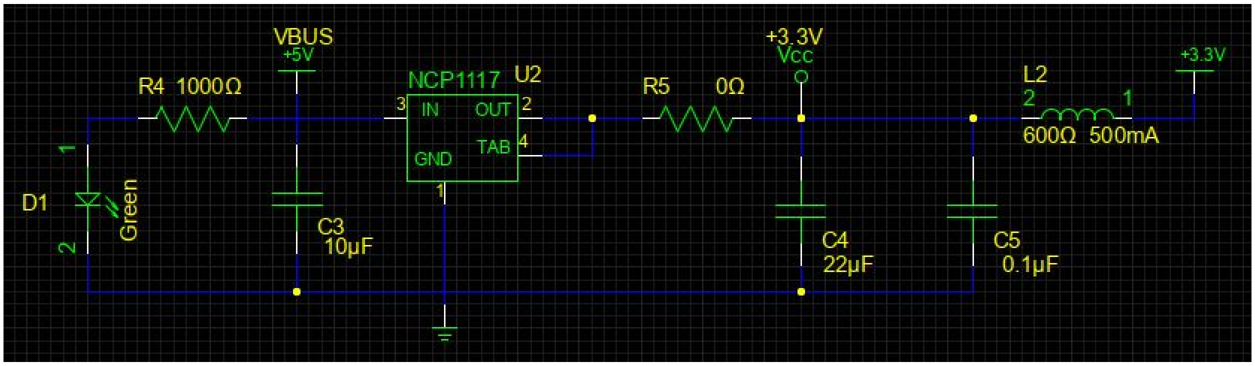


Fig. 24 - Schematic diagram for regulator, +3.3 V Main.

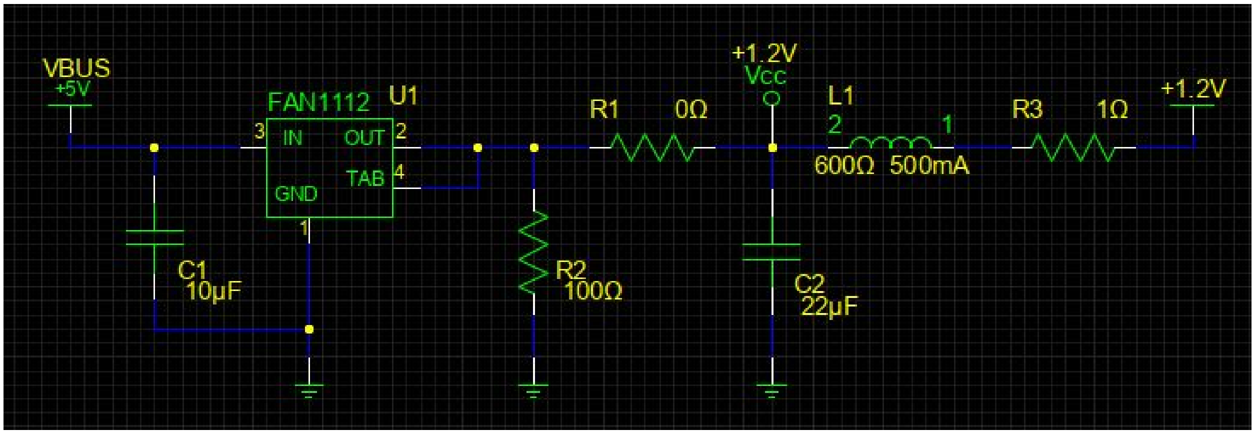


Fig. 25 - Schematic diagram for regulator, +1.2 V CPLD.

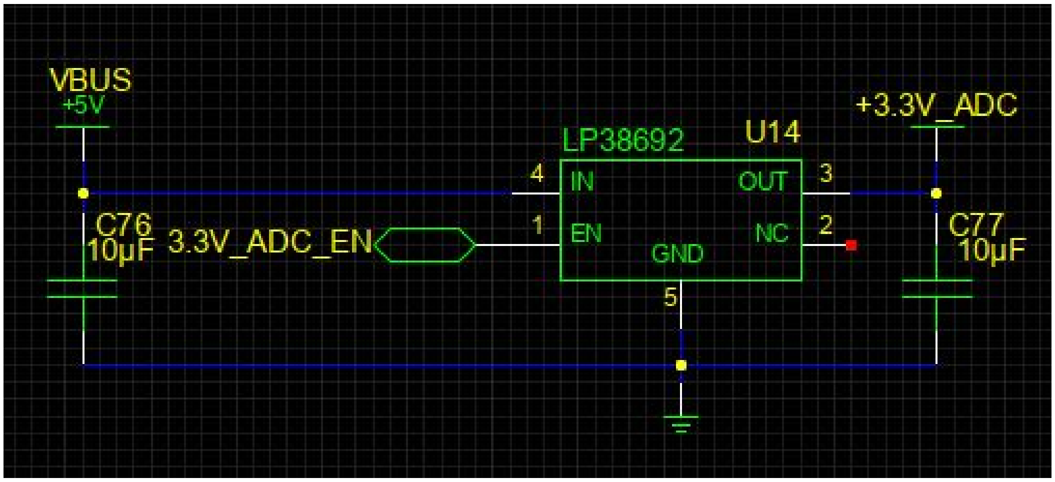


Fig. 26 - Schematic diagram for regulator, +3.3 V ADC.

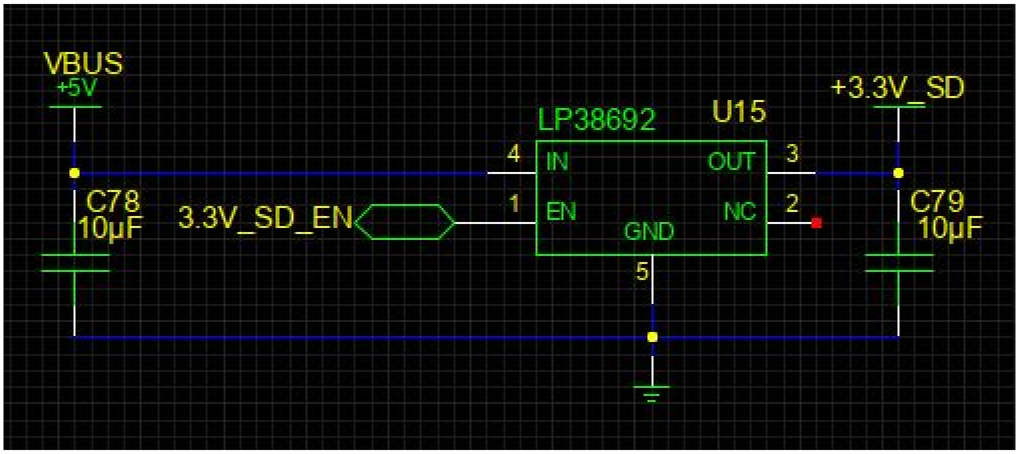


Fig. 27 - Schematic diagram for regulator, +3.3 V SD.

4.3 Additional Schematic Diagrams

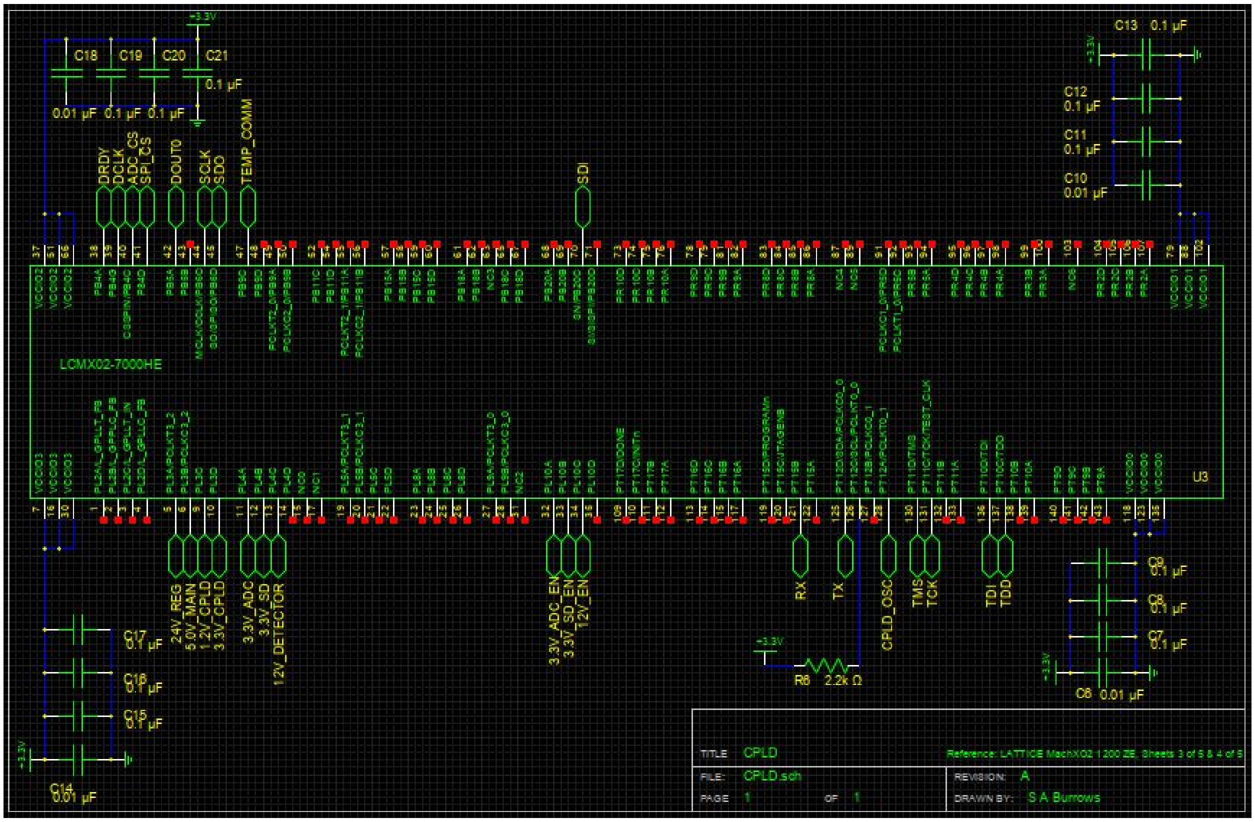


Fig. 28 - Schematic diagram for the CPLD.

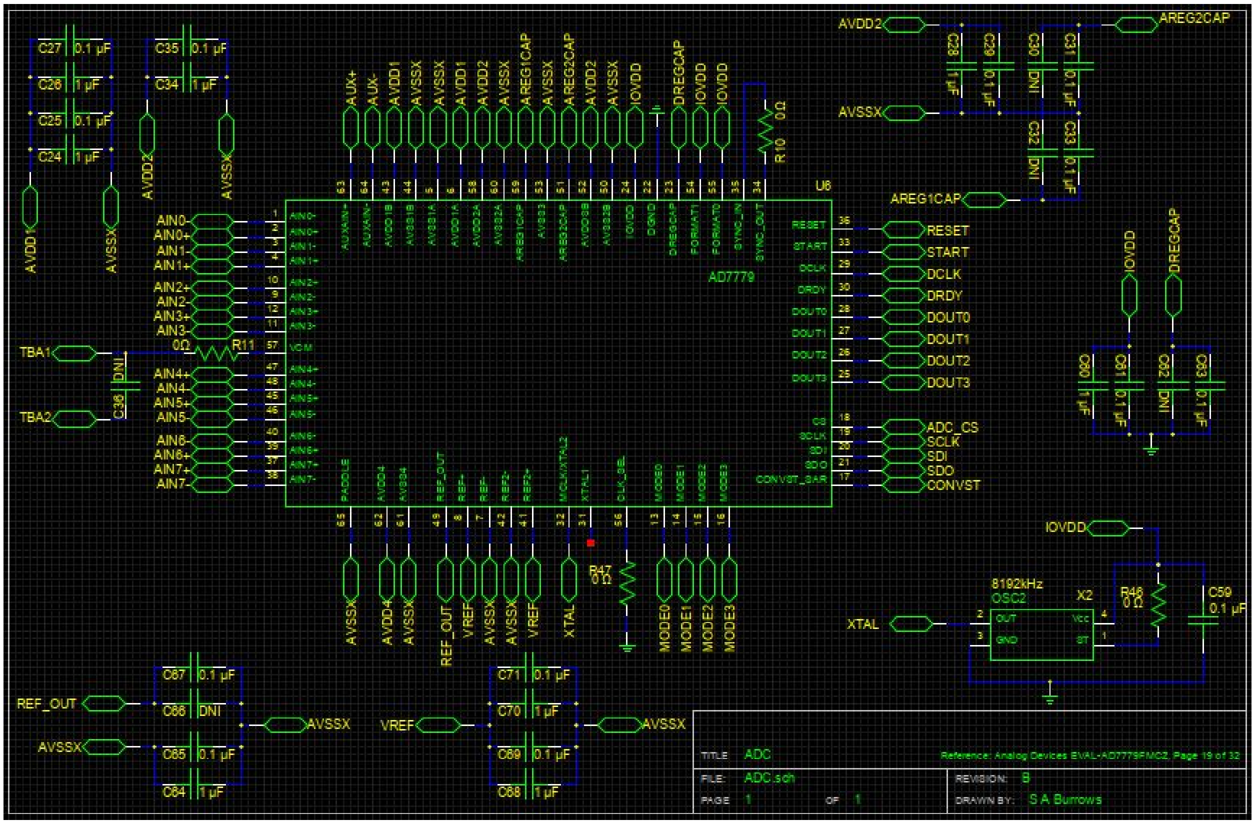


Fig. 29 - Schematic diagram for the ADC circuit, with oscillator.

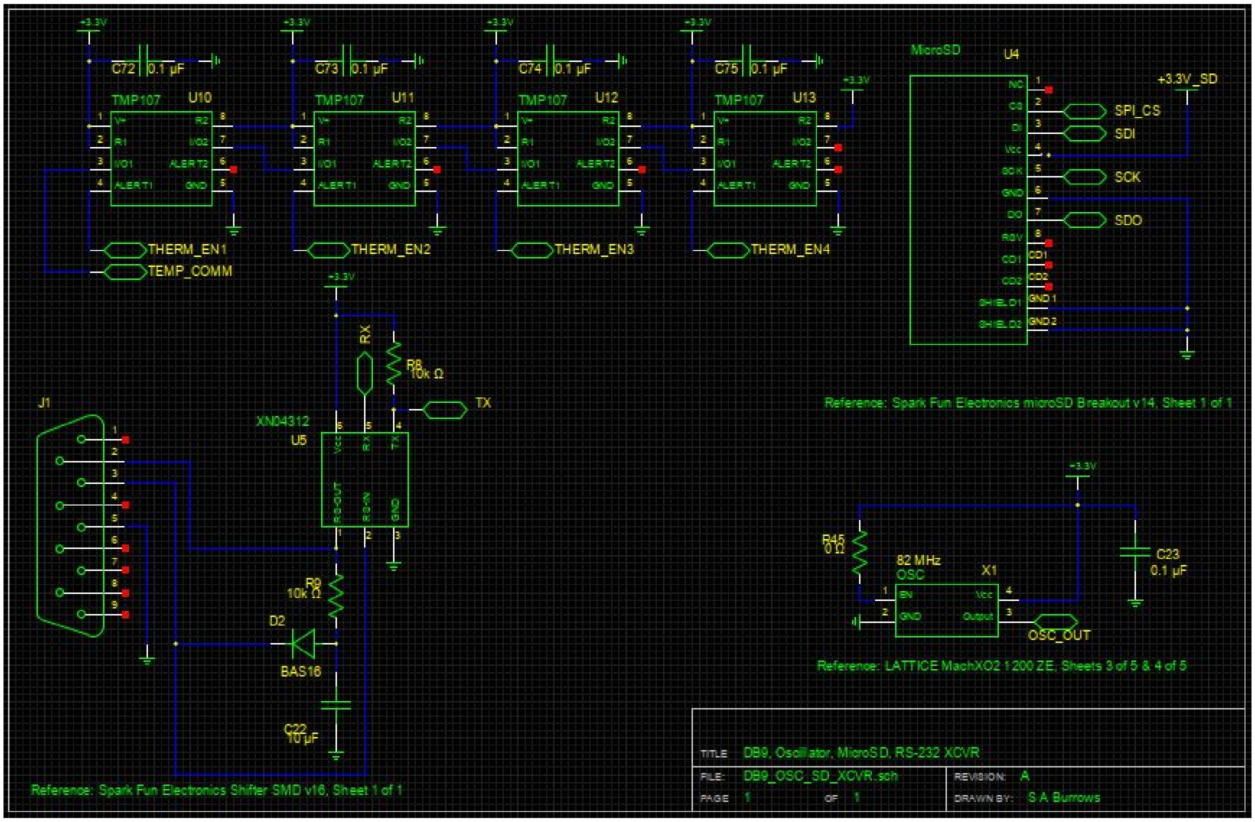


Fig. 30 - Circuits for temperature sensors, CPLD oscillator, RS-232, and SD card.

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