

HASP 2013 Final Science Report and Failure Analysis



Montana State University
Payload 04
“Single Event Effect Detector”

December 13, 2013



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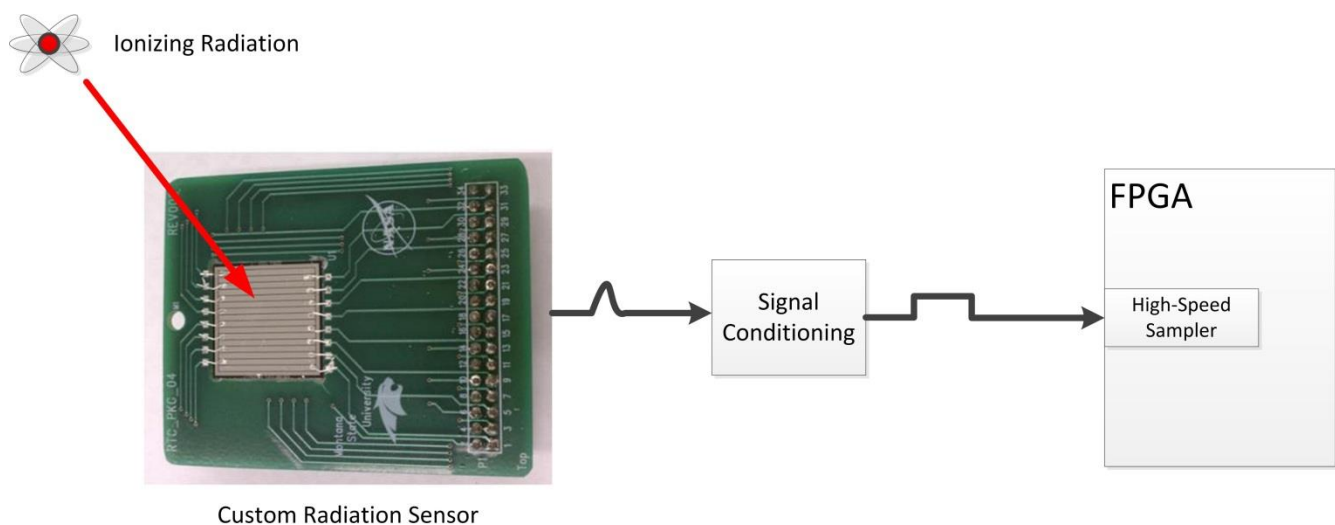
I. Introduction

The Single Event Effect Detector has been designed and developed as part of ongoing research at the Montana State University High-Speed Digital Design Lab in Bozeman, Montana. The overarching goal of this research is to demonstrate a radiation-tolerant, SRAM-based FPGA computer system capable of operation in harsh terrestrial or space radiation environments. As with most electronics designed for these types of applications, this system seeks to mitigate single event effects caused by the interactions between ionizing radiation and modern electronics. “Single event effects” is an umbrella term for several possible scenarios involving these interactions. As a high-energy particle passes through a semiconductor material it leaves behind a charge track consisting of electron-hole pairs. In the context of the affected electronic system, the recombination of this excess charge represents an errant electrical current. A single event transient (SET) occurs when this current flows in such a way as to cause a transistor to temporarily change state. If perchance this erroneous transient state is latched into a memory element within the system, a single event upset (SEU) occurred. The behavior of SRAM-based FPGAs is determined by radiation susceptible memory contents. An SEU occurring within this memory changes the functionality of the underlying hardware, and is known as a single event functional interrupt (SEFI). Many techniques exist for mitigating these effects. These techniques frequently combine shielding with redundant hardware systems wherein the shielding reduces the amount of radiation that reaches the sensitive electronic components and the redundant hardware prevents errors from propagating through the computer system. Additionally, manufacturing processes may be used to increase radiation tolerance at the chip level often at the expense of circuit performance and higher cost. The flexibility of FPGAs can be leveraged to implement radiation tolerant architectures on-chip using coarse-grained triple modular redundancy (TMR) along with majority-rules voting. Readback scrubbing of the configuration memory combined with the ability to dynamically reconfigure regions within the FPGA at runtime can be used to enhance radiation tolerance.

The effects of ionizing radiation are largely absent on the earth's surface due to the combined shielding of the magnetosphere and atmosphere. This makes testing radiation tolerant computer architectures difficult due to the lack of single event effects. There are only a handful of ways to test space-bound systems on earth. Sophisticated high-energy pulsed laser systems and particle accelerators, both of which are expensive and pose logistical difficulties when testing electronic components, are among the testing options. High-altitude scientific balloons offer a unique platform for testing radiation effects. Though the radiation levels in the near-space atmosphere are lower than would be found in space, they tend to be significantly higher than on earth's surface. Scientific

balloons enable systems to be tested in harsh radiation environments for longer durations than suborbital launch vehicles, and, in the case of the HASP program, at significantly reduced cost.

The payload designed for the HASP 2013 flight was a first-generation general purpose test platform for FPGA-based radiation-tolerant computer architectures. The payload electronics consisted of a custom printed circuit board stack. The circuit boards populated for flight included a power supply board, an FPGA computer board, and radiation sensor boards. In addition to serving as a radiation tolerant hardware test platform, the FPGA board was a data logger for the radiation sensors. The sensor was a custom silicon strip sensor which was designed and built in-house by researchers at Montana State University. The 18-mm x 18-mm sensor is comprised of 16 front-side detection channels and 16 back-side detection channels. The front- and back-side channels are oriented orthogonally to create a 256-intersection grid. The sensor outputs were monitored by high-speed sampling logic within an FPGA.



The radiation sensors were designed for inclusion in the PCB stack in order to provide an environmental awareness to control-elements of the computer architecture. This is meant to help detect and prioritize the repairing of faults. This report details the science objectives for this payload on the HASP flight, the concept of operation, the enabling hardware platform for this research and results from the 2013 flight.

Figure 1- Radiation sensor signal path

II. Science objectives

II. a. Radiation sensor testing

The primary science objective for this flight was to demonstrate the functionality of the radiation sensors in a near-space environment. The high altitude and extended duration of the HASP flight offered a unique opportunity to test the sensor under exposure to cosmic radiation. The chance of observing strikes by radiation with enough energy to pass fully through the sensor was increased by the long flight duration. Particles which pass completely through the 300- μm thickness of the sensor are of particular importance because they register in the high-speed sampling circuitry as intersections of front and back-side sensor channels. Strikes which only register on a front side channel are assumed not to have passed through the sensor, and therefore they do not pose a threat to the computer system. Data from intersection strikes, including the rate at which they occur, can subsequently be input into fault injection simulations to extract worst-case scenario performance statistics of radiation-tolerant computer architectures. Neutrons were expected to be the predominant particles encountered as they represent the bulk of energetic particles in the atmosphere (1). The atmospheric neutron flux is well known (2) and a major test of the sensor was to replicate the neutron flux profile during the ascent phase of the flight. The desired data products included the ionizing radiation strike rate (particles/s), sensor spatial strike information, and particle flux (particles/cm²/s).

II. b. SEE detection in SRAM FPGAs

A secondary science objective was to detect single event effects within either of the two FPGAs in the payload. This objective required the complete design and development of the radiation-tolerant architecture test platform. The FPGA board was designed to include two FPGAs: a control FPGA, and a general-purpose, high-performance computational-resource FPGA. The control FPGA, a Xilinx Spartan-6 (XC6SLX75), acted as a system controller as it housed the high-speed sampler for the radiation sensor, controlled the communication between the payload and the HASP platform, and controlled the configuration and operation of the computational FPGA. The computational FPGA was a Xilinx Virtex-6 (XC6VLX75T-1L). The 2013 flight expanded on the 2012 system by implementing a complete radiation hardened FPGA computer platform with on-chip TMR and scrubbing to mitigate the radiation induced errors should one have occurred.

For the HASP 2013 flight, the Spartan-6 device used a dedicated, internal CRC hardware component on the configuration memory, which was input into the control microprocessor as an interrupt to indicate fault occurrence. The SEE detection strategy for the Virtex-6 used an array of 9

MicroBlaze processors with three running at a time (triple modular redundancy, or TMR). The outputs of the processors were sent to a majority voter, which determined if any of the active processors were faulted. The system would replace faulted processors with one of the available spares. Signals representing the set of active processors were sent to the Spartan-6. Single event effects could thus be observed through changes in the active processor set in the Virtex-6.

II. c. Thermal performance

A third science objective, which evolved over the life of the project, was to determine the thermal behavior of the electronics in a low-pressure environment. As our hardware was relatively unchanged from the 2012 flight, we based our predictions and thermal design on the successes of this flight. The payload enclosure was designed with the main goal of maintaining FPGA core temperatures within their specified operating ranges. The inability to cool the electronics using convective processes complicated the design. A combination of conduction and radiative cooling were used to move heat away from the electronics and radiate it externally through the base plate to earth. The complicated the thermal behavior of the system during the integration testing, but was very effective during actual flight operations.

III. Concept of Operation

The payload was designed for autonomous flight operation with minimal administrative commands. At power-on, the system performed an initialization sequence during which the FPGAs were configured, the control processor was booted, and the data storage structures were initialized. A MicroBlaze soft processor was used to control the system. Its operation was interrupt-driven as it handled receipt of commands and GPS data from the HASP platform, and transmitted raw telemetry data at each expiry of a 60-second fixed-interval timer. Transmitted data included a system counter, which served as a heartbeat to show that the system was running, the number of cumulative counts observed on each channel of the radiation sensor, the junction temperature of the Virtex-6 FPGA, GPS time and position data, single event effects data, and system status flags.

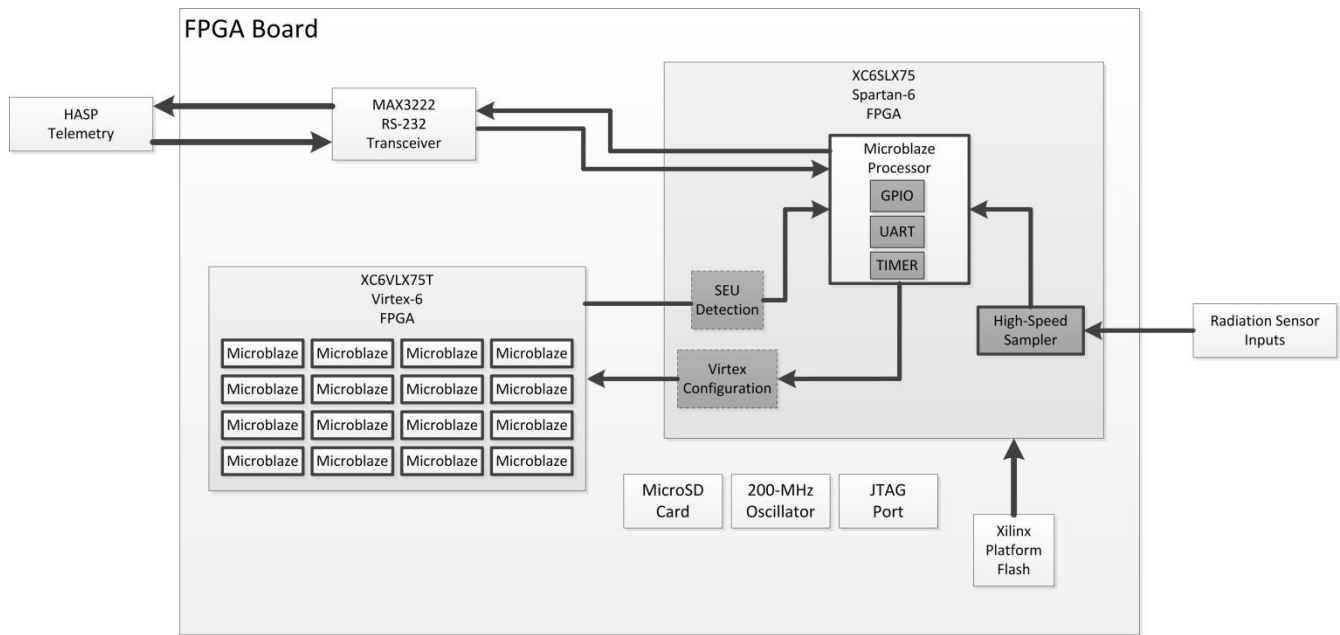


Figure 2- FPGA CCA architecture. This figure shows 16 MicroBlaze processors instantiated on the Virtex-6, the RS-232 interface to the HASP platform, and the major components of the MicroBlaze processor on the Spartan-6 FPGA.

The data were retrieved from the HASP website as it became available during the flight. After retrieval, the data were processed in a C# GUI or MATLAB and the contents of each telemetry packet were displayed on a graphical user interface. This gave the team the ability to scroll through all the received packets to determine how the system was operating. Two payload commands were available to the team during the flight. These were commands to reset the radiation sensor counters and to reconfigure the Virtex-6. The primary job of the team during the flight was to make sure the payload was transmitting data as expected.

IV. System Hardware

IV. a. Power CCA

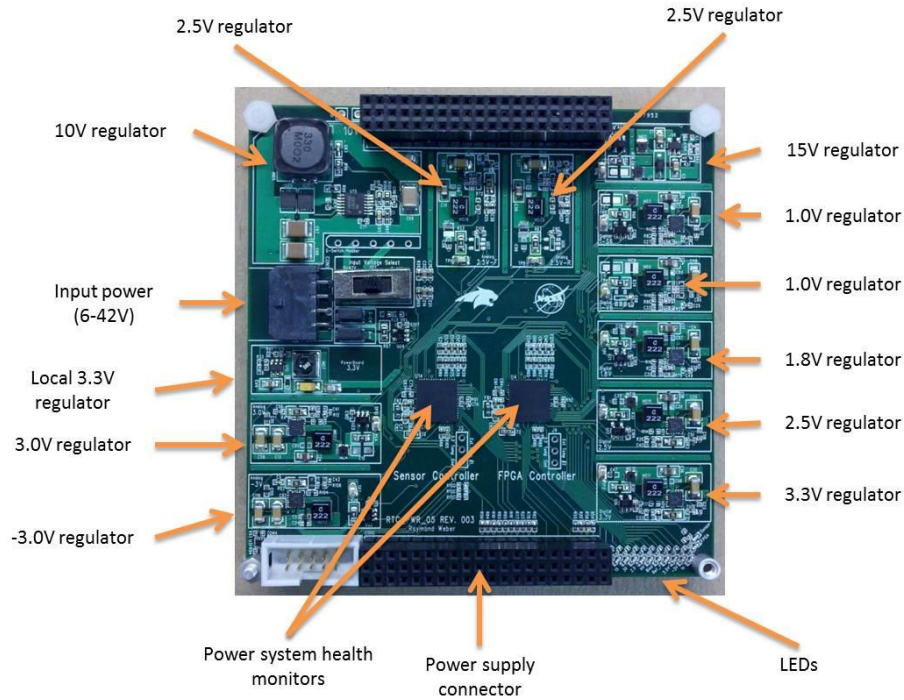


Figure 3- Power CCA designed for the HASP 2013 flight.

Power was supplied to the payload via the HASP interface. The Power CCA, shown in figure 3 generated the required internal system voltages from the provided 30 ± 2 volt supply. Given the strict power consumption restrictions the system was designed using high-efficiency DC-DC converters. This minimized the amount of the payload power budget consumed by the conversion process. A secondary benefit of efficient power conversion is a reduction in generated heat as compared to linear regulators. The FPGA CCA and sensor electronics combined to require 10 voltage rails, 1 intermediate rail and 1 rail internal to the Power CCA for the system monitors. This year we added independent supplies for the analog comparators and sensor bias allowing these values to be modified easily with only software modifications and reduce noise between the analog and digital circuitry. The measured power consumption at payload integration was 7.4 watts. Fitting this number of regulator circuits on the 4-in x 4-in PCB required careful design work. A diagram detailing the conversion architecture is shown in figure 4.

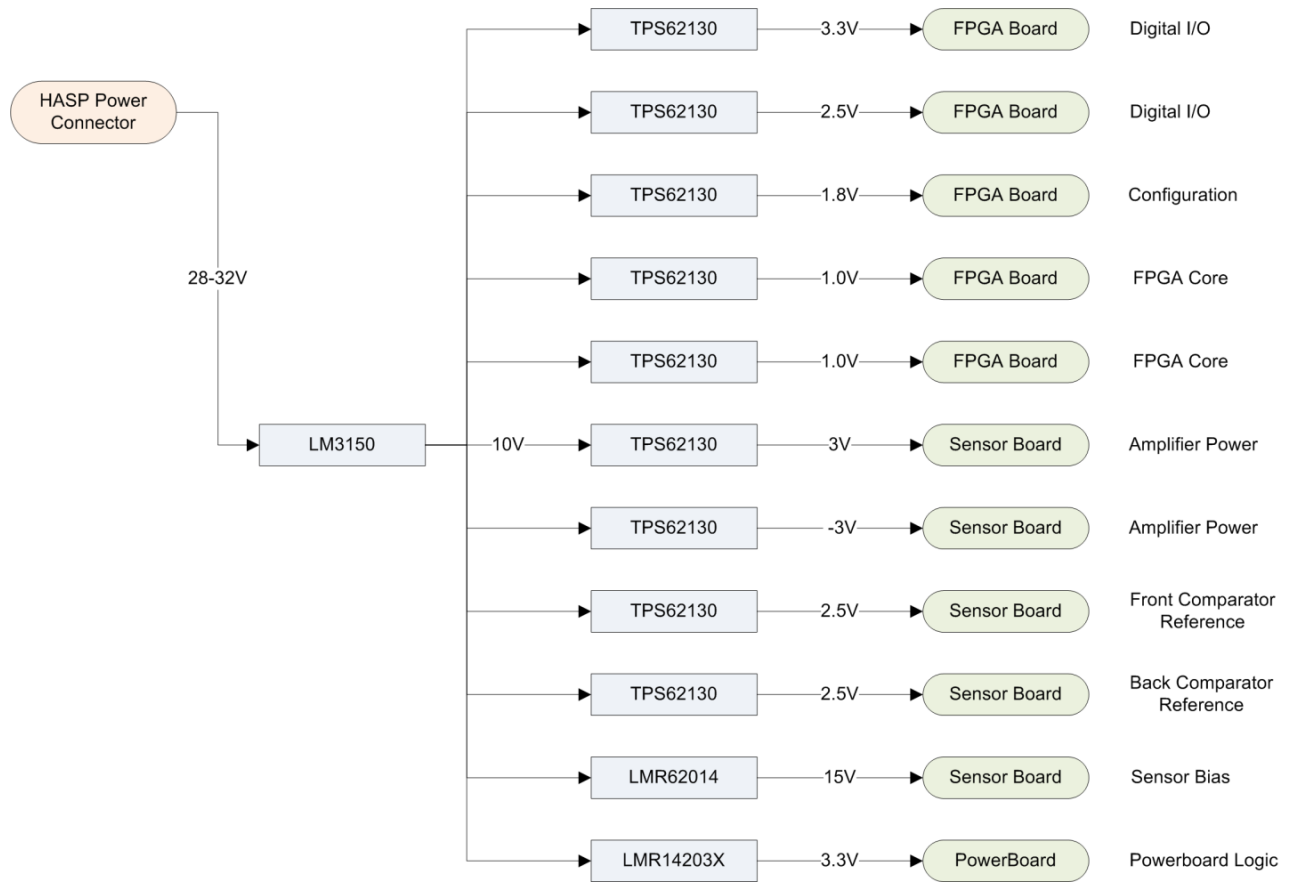


Figure 4- Power conversion diagram.

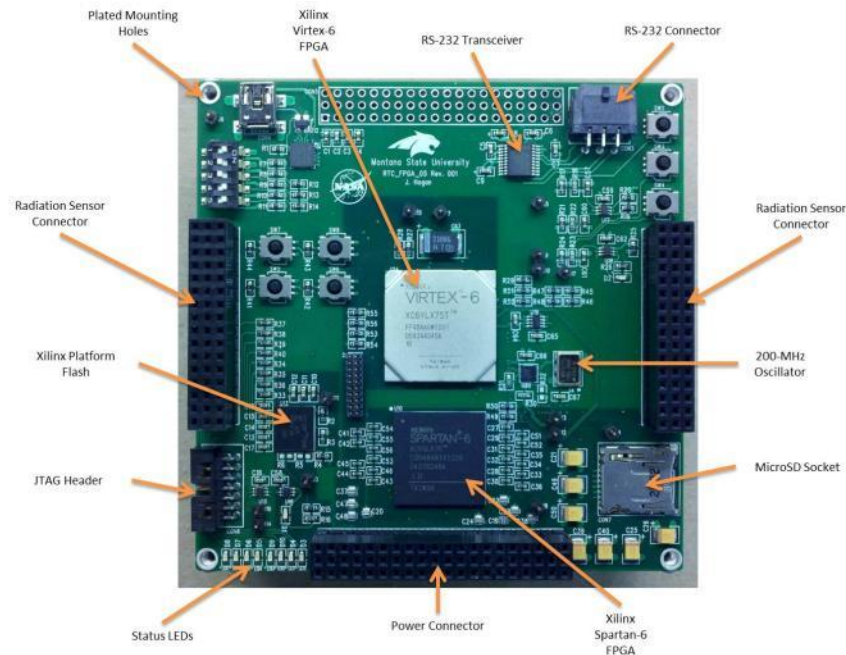
IV. b. FPGA CCA

Figure 5- FPGA CCA designed for the HASP 2013 flight.

The FPGA circuit card assembly served as the system controller for the flight and its hardware was unchanged from the 2012 flight. Upon application of power to the payload, the Spartan-6 FPGA self-configured using an 8-bit SelectMAP Master interface to a 32-Mbit configuration memory device. The Spartan-6 FPGA contained three major hardware components: an SD card controller, a MicroBlaze soft processor, and the high-speed radiation sensor sampling logic. Immediately after configuration, the SD card controller performed an initialization sequence on the SD card to allow access to it via an SPI interface. The SD card was pre-loaded with the configuration bitstream for the Virtex-6. Once the SD card initialization process was complete, control of the card was handed over to the processor. The first task of the processor was to read the configuration data from the SD card and write it to the Virtex-6 via an 8-bit SelectMAP Slave interface. Upon completion of the configuration process, the processor began data collection operation. The process was interrupt driven and had service routines for the following tasks: read commands and GPS data from the HASP RS-232 interface, transmit command receipt acknowledgments to the HASP RS-232 interface, record CRC error in configuration memory contents, and transmit telemetry packet every 20 seconds. As part of the telemetry transmission task, the processor would read the most recent GPS location and time data, the junction temperature of the Virtex-6 and the contents of the radiation sensor sampler memory. Each valid telemetry packet was 1224 bytes long including a header, footer, checksum, and all data contents.

IV. c. Sensor CCA

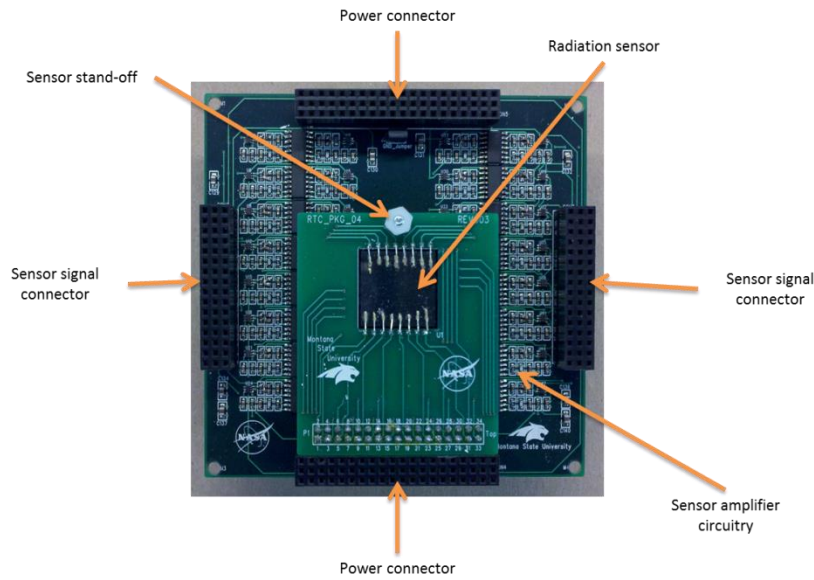


Figure 6- Radiation sensor CCA. The CCA includes the radiation sensor, sensor signal breakout board, and signal conditioning electronics.

The radiation sensor CCA consists of a custom silicon strip sensor and a chain of amplifiers used to condition the analog sensor outputs into a square pulse. The radiation sensor is a silicon-based strip detector. The substrate consists of an intrinsic silicon wafer with a P-type (Boron doped) front surface and an N-type (Phosphorous doped) rear surface. These doped regions produce an inherent electric field inside of the silicon sensor. When a heavy radiation particle penetrates the sensor, bonds between electrons and host atoms are broken. The breaking of these bonds produces free electrons inside the substrate. The movement of these electrons effectively produces two types of charge carriers. The electrons themselves are the first carrier. The second carrier is represented by the void left by a traveling electron and is known as a hole. The combination of the traveling electrons and holes produces the desired signals. Once these carriers are generated, they are separated by the internal electric field inside the sensor. The electrons are pushed to the rear of the sensor while the holes move towards the front. These transient signals are then collected from the front and rear aluminum electrodes. The signals are input into a two-amplifier chain which amplifies and stretches the pulse for input into the high-speed sampler located in the Spartan-6. The high-speed sampler is a rising-edge triggered system which functions as a counter for each of the radiation sensor channels.

IV. d. Electronics Stack

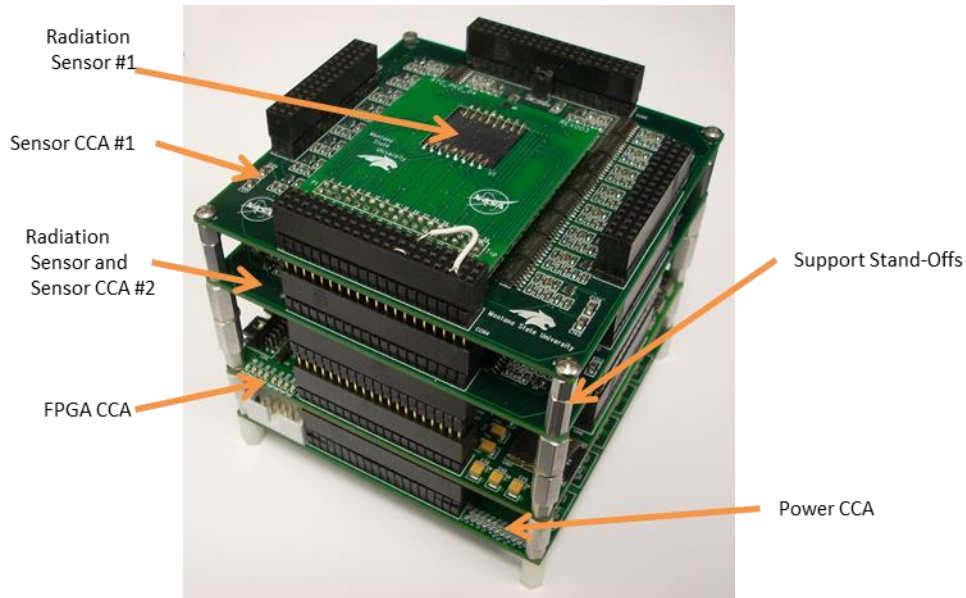


Figure 7 - Payload electronics stack.

The payload electronics stack consisted of a Power CCA, an FPGA CCA and two Sensor CCAs. The circuit boards were stacked together using through-hole connectors and secured using threaded aluminum stand-offs at each corner. In addition to providing mechanical support these stand-offs were part of the payload thermal solution. The mounting holes on the FPGA and Power CCAs were plated and connected to the internal ground planes. This allowed heat to flow through the PCB ground planes to the aluminum stand-offs. A 4x4x1/8-in copper plate was placed at the bottom of the payload, secured using the stand-offs, and used as a heat sink during flight. Thermal models indicated this was a good solution for maintaining the desired operating conditions, and the payload encountered no thermal issues during payload integration or flight.

IV. e. Enclosure

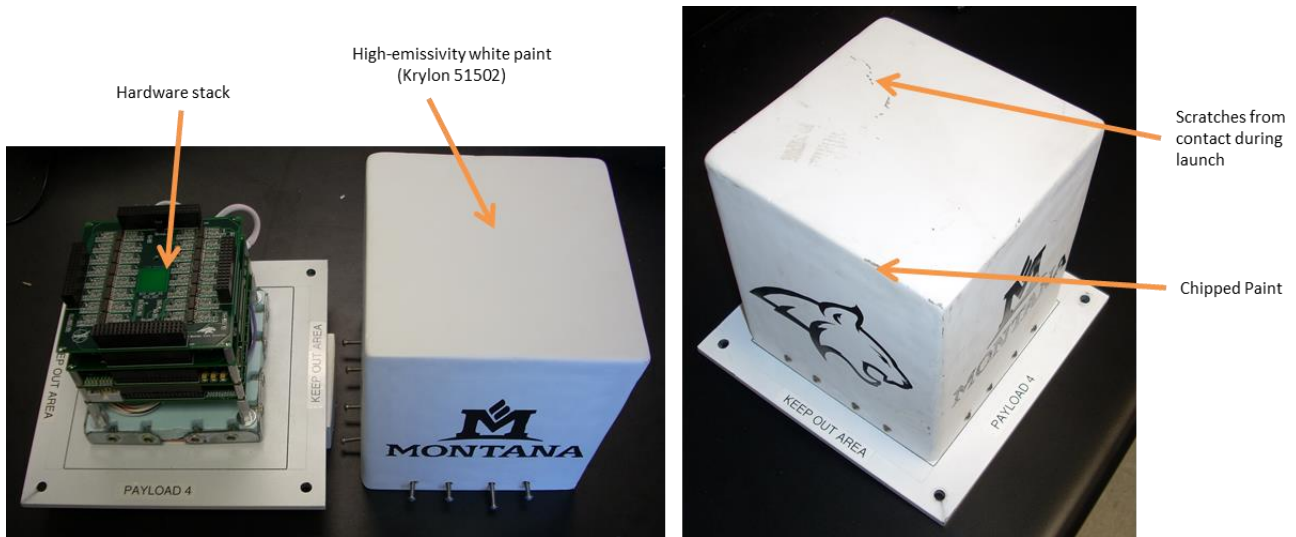


Figure 8- Payload enclosure. The enclosure was made of half-inch thick foam insulation wrapped in a thin sheet of aluminum foil. A fiberglass layer was added for structural support. The enclosure was painted using Krylon Indoor/Outdoor Flat White spray paint (#51502).

The enclosure was designed for thermal and mechanical protection of the payload electronics. The approach to thermal protection sought to maximize reflection of solar irradiation using a thin layer of aluminum and a flat, high-emissivity white paint. Beneath the aluminum layer was a half-inch of insulating foam material, which minimized heat transfer between the enclosure and the outside environment. Within the enclosure, the heat generated by the electronics was conducted away from sensitive components through PCB ground planes, into aluminum support stand-offs, and into a copper heatsink. The heatsink was placed inside the enclosure, beneath a piece of insulating foam to prevent internal radiative heat transfer. The bottom of the heatsink was in contact with the PVC mounting plate. Though not an excellent thermal conductor, it was expected that this configuration would heat the mounting plate allowing a moderate amount of heat to be radiated from the payload toward the earth. The electronics stack and enclosure were attached to the mounting plate separately. The electronics stack was secured by screws which engaged the threaded aluminum stand-offs. The enclosure was held in place using bolts and nuts which affixed internal angle brackets to the mounting plate. The enclosure survived the flight very well. Damages to the payload between launch and return shipment receipt included chipped paint on the enclosure lid and some paint scratches that we attribute to the payload striking the crane during launch.

V. Results

The following table provides an events timeline for the payload during the flight. The payload operated nominally during the entire flight and required no intervention or power cycles.

Event	Time (MDT)	Description
Initial Power-On	07:53	Payload turned on for flight
First Data Packet	07:53:44	First Packet Timestamp
Launch	08:54:44	
Start of Float Period	10:55:44	Balloon reached float altitude
Last Data Packet	21:07:44	Final Packet Timestamp
Flight Termination	21:25:22	
Impact	22:10	HASP platform back on the ground

Table 1 - Major events during the flight.

As the data became available during the flight it was processed and viewed in a custom telemetry GUI. This GUI provided a graphical display of the radiation sensor including the number of cumulative strikes at each of the 256 intersections. In addition to the radiation sensor data, the GUI displayed the contents of the most recent telemetry packet. This included the system heartbeat counter, UTC time, latitude, longitude, altitude, GPS fix status, a payload start status word, the set of active processors on the Virtex-6 and the Virtex-6 junction temperature. Figure 9 below shows the data processing GUI.

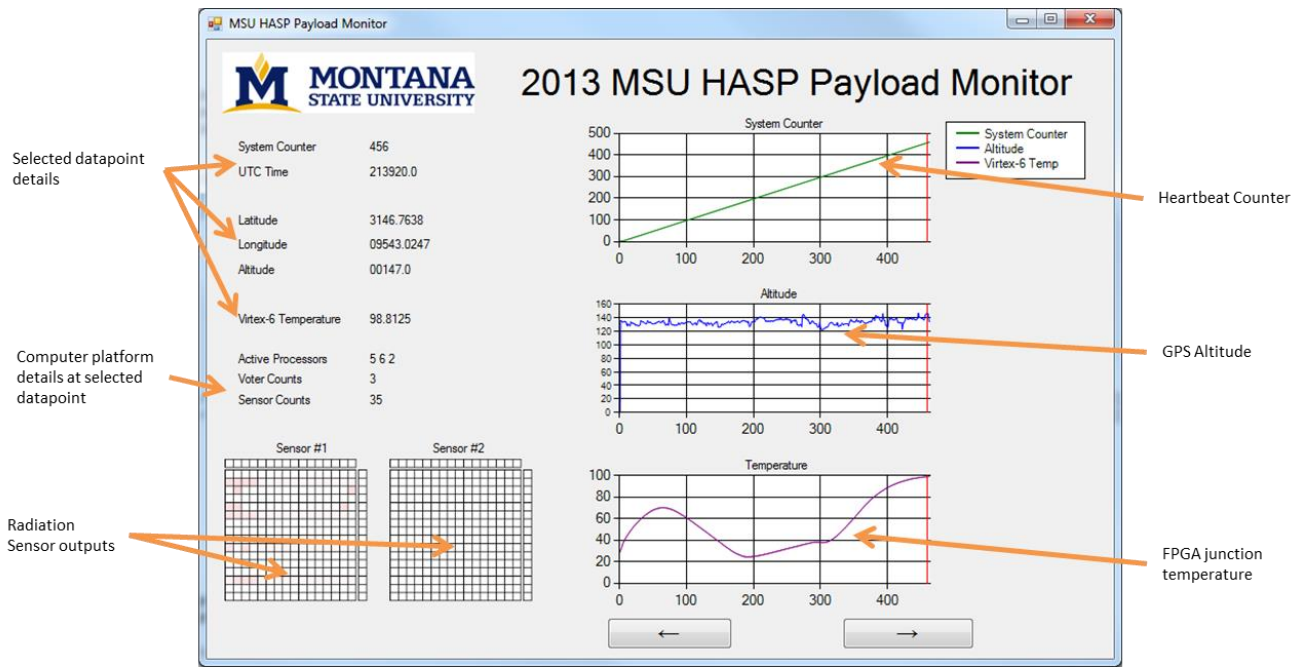


Figure 9- This figure shows the data processing GUI used during the flight. The presentation of the telemetry data simplified the monitoring of payload operation.

The SEE detection circuitry worked throughout the flight without detecting any events. This scientific objective was considered secondary science due to the small, though non-zero, chance of observing an upset in a sensitive bit within either of the FPGAs. The chance of upset was considered small due to the low SEU cross-section of the FPGAs (on the order of 10^{-9} cm²/bit) (3) as well as the expected low bit error rate. Bit error rates are low because of the combination of a negative correlation of particle flux with particle energy and small radiation cross-section of the devices. Only a handful of particles with sufficient energy to induce an upset were expected to be encountered during the flight, and these particles needed to strike the FPGA substrate in very specific locations to be observed. The effects of high-energy particles on avionics is well known (2,4,5,6), so with this flight hardware an attempt was made to detect these effects despite the low probability of occurrence.

The radiation sensor system logged the cumulative number of strikes observed on each channel during the flight. Some interesting behavior patterns were observed in the data. For the majority of the flight the sensor was idle, observing no radiation strikes. Upon system power-up, and prior to launch, the sensor counts were observed increasing exponentially. This exponential rise in counts closely mirrored the measured payload internal temperature. After further study, it was found that the sensor counted whenever the payload temperature was increasing, and ceased counting when the temperature

was steady or decreasing.

In an effort to isolate radiation strikes from the observed thermal effects, the difference between count values for each packet was plotted. This enabled a quick visual inspection of when events occurred on a given channel. By also plotting system temperature with the sensor counts individual events could be isolated and studied. Small increments in radiation strike counts under steady or decreasing temperature conditions were considered most likely to be radiation strikes. Figure 10 shows the results for one of the 16 channels for each sensor during the flight.

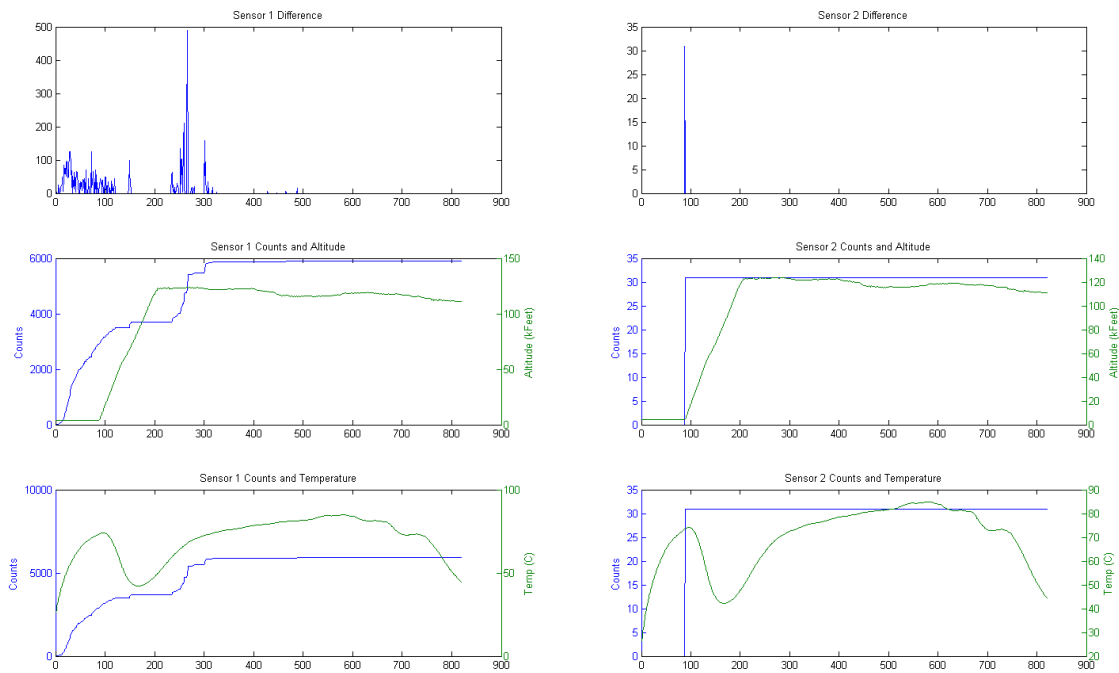


Figure 10-- This figure shows differential count values versus time in the top two plots. Cumulative count values and altitude versus time are shown in the middle plots. Cumulative count values and temperature versus time are shown in the bottom plots.

To visualize the data for an entire sensor through the duration of the flight a 3-axis plot was created. This plot shows the cumulative count values for each channel versus time. The surface represents the number of strikes on a given channel at a given time. For the sensor shown in Figure 11, the several major events were observed.

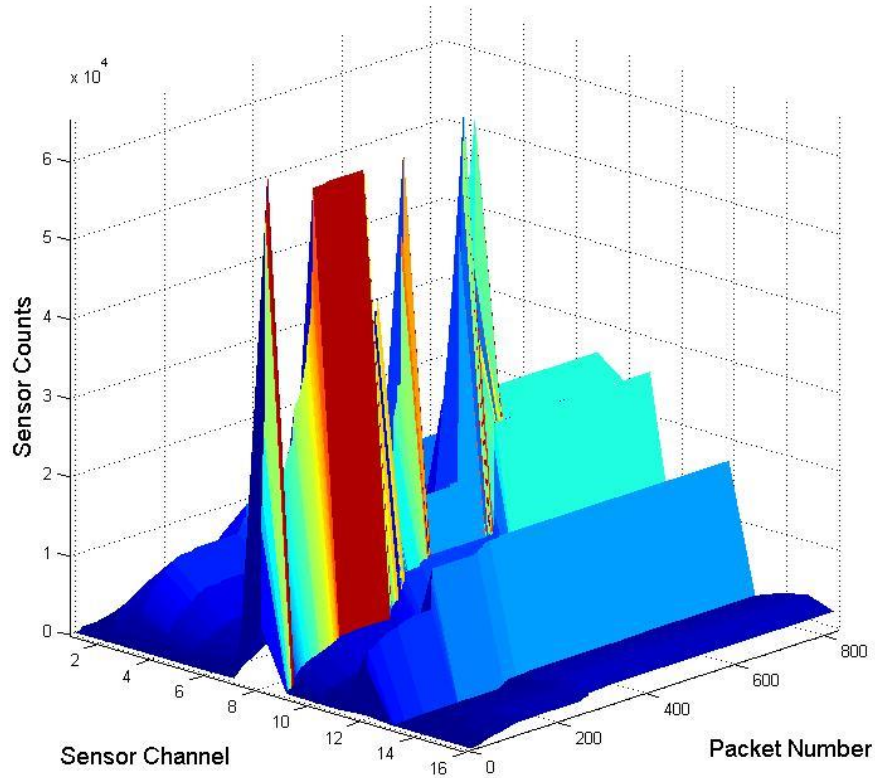


Figure 11-- This figure shows a surface plot representing the cumulative sensor counts for each channel as a function of time.

VII. Team members and demographics

VII. a. Participant demographics

Name	Gender	Ethnicity	Race	Student Status	Disability
Blaine Ferris	Male	Non-Hispanic	Caucasian	Undergraduate	No
Justin Hogan	Male	Non-Hispanic	Caucasian	Graduate	No
Sam Harkness	Male	Non-Hispanic	Caucasian	Graduate	No
Raymond Weber	Male	Non-Hispanic	Caucasian	Graduate	No

VII. b. Recent graduates

Todd Buerkle – MSEE, May 2012, Micron Semiconductor, Product Engineer

Elizabeth Clem – BS Mechanical Engineering Technology, May 2012, employment unknown.

Jennifer Hane – MSEE, May 2012, Seakr Engineering, FPGA Engineer

Adrien Lambert – MSME, December 2012, employment unknown

VIII. References

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