I. Executive summary

I. a. Scientific objectives summary

- Measure atmospheric radiation flux profile using a custom silicon strip radiation sensor
- Flight test a radiation-tolerant computer architecture implemented on non-hardened SRAM-based FPGAs.
- Demonstrate use of radiation sensor to provide an environmental awareness to the radiation-tolerant computer architecture.

Resource	Usage Estimate
Weight	1.7-kg
Height	б-in
Footprint	5.8 x 5.8-in
Power	7-W
Current @ 30-V	220-mA
Serial uplink commands	Infrequent, as-needed
Downlink telemetry	Periodic packet with checksum
Downlink bit rate	518-bps
Analog channels	none
Discrete commands	none
Payload location and orientation	any

I. b. HASP resource utilization estimates

II. Payload description

II. a. Introduction

The payload proposed herein is a follow-on to the Montana State University (MSU) payload flown in the HASP 2012 program and continues the work performed as part of that effort. The 2012 payload fell short of accomplishing the scientific objectives for which it was designed. These shortcomings are detailed in the final science report/failure analysis submitted for the 2012 project. Major hardware design was undertaken in the 2012 payload effort resulting in the development of a highly flexible computer architecture test platform. The majority of the project schedule was consumed by PCB design with delivery of the completed electronics coming in late June. This left just over a month for the full payload design to come together including a first power-on test of the power supply board and the dual-FPGA computer board, software development, system testing and enclosure integration. Fortunately, all of this went smoothly and the payload was integrated and flown. The 2012 flight exposed several minor design flaws; two of which prevented the fulfillment of the primary science objectives. These flaws have been studied and corrected, and continued testing will help ensure successful system performance on any subsequent flight opportunities. Though the science objectives were not met, the undertaken design effort has left the research group poised to re-deploy an improved system. With the electronic hardware design out of the way, significantly more time can be devoted to research and science aspects of the project. More time is available for FPGA system design, radiation sensor gain calculation/calibration, software development, data processing preparation, and rigorous testing of the full payload system prior to HASP integration and flight.

II. b. Scientific Objectives

II. b. 1. Radiation sensor testing

The primary science objective for this flight is to demonstrate the functionality of the radiation sensor in a near-space environment. The high altitude and extended duration of the HASP flight offers a unique opportunity to test the sensor under exposure to cosmic radiation. The chance of observing strikes by radiation with enough energy to pass fully through the sensor is increased by the long flight duration. Particles which pass completely through the 300-µm thickness of the sensor are of particular importance because they register in the high-speed sampling circuitry as intersections of front and back-side sensor channels. Strikes which only register on a front side channel are assumed not to have passed through the sensor, and therefore

do not pose a threat to the computer system. Data from intersection strikes, including the rate at which they occur, can subsequently be input into fault injection simulations to extract worst-case scenario performance statistics of radiation-tolerant computer architectures.

Neutrons are expected to be the predominant particles encountered as they represent the bulk of energetic particles in the atmosphere (1). The atmospheric neutron flux is has been studied (2) and a major test of the sensor is to replicate the neutron flux profile during the ascent phase of the flight. A profile similar to the one shown in (2) for 1-10 MeV neutrons is expected to be measured by the radiation sensors. The desired data products include the ionizing radiation strike rate (particles/s), sensor spatial strike information (strike location), and particle flux (particles/cm²/s). The payload will include two radiation sensor boards. This science objective will be performed using carefully selected amplifier gain values which are great enough to measure the low energy portion of the radiation environment.

II. b. 2. Flight testing of a radiation tolerant computer system

A second science objective for this flight is to test a radiation tolerant computer architecture. This architecture leverages the performance and flexibility of off-the-shelf SRAM-based FPGAs to detect, avoid, and repair single event effects caused by ionizing radiation. Fault detection is performed in two ways: at runtime through the use of coarse-grained triple modular redundancy (TMR), and through readback and scrubbing of the FPGA configuration memory, using strike detections from the radiation sensor to guide the scrubbing effort. The FPGA logic fabric is divided into nine independent computational tiles. Each tile contains a Microblaze processor running a software algorithm. Three of the tiles are members of an active triad in a TMR implementation. Their outputs are routed through a multiplexer to a majority-rules voter that determines a valid output and prevents erroneous outputs from propagating through the system. The remaining six tiles are held in reset and are available as spare processors. Should one member of the active triad become faulted, a spare tile is quickly brought on line in place of the faulted tile. In this way, system operation can continue with minimal interruption and the fault is avoided. Each computational tile is partitioned as a reconfigurable region allowing reconfiguration at runtime without affecting neighboring tiles. This allows spare tiles to be maintained and faulted tiles to be repaired in the background while the active triad performs the desired system function. Though they don't occur frequently, several upsets can reasonably be expected over the course of a 7+ hour flight at high altitude. This expectation is based on the

well documented radiation effects on avionics (1,2,4,5,6). Even if faults occur in non-critical regions of the FPGA design and don't impact system operation, they will still be logged as FPGA upsets. This allows the entire FPGA to be used as a single event effect detector and the radiation tolerant computer architecture to be tested simultaneously. The radiation sensor used to support this science objective will have a lower associated gain values to prevent response to particles without sufficient energy to penetrate into the FPGA.



II. c. Payload Systems

II. c. 1. Power CCA

Figure 1- This figure highlights the main features of the Power CCA. This hardware is a second revision based on the hardware flown on the HASP 2012 flight. The dimensions are 4-in by 4-in.

The Power CCA generates the required internal system voltages from the provided $30\pm 2V$ supply. Given the strict power consumption restrictions the system was designed using high-efficiency DC-DC converters. This minimizes the amount of the payload power budget consumed in the conversion process. A secondary benefit of efficient power conversion is a reduction in generated heat as compared to linear regulators. The Power CCA generates the eight voltage rails required by the FPGA CCA and Sensor CCAs. One intermediate 10V rail is

also generated to increase conversion efficiency of the lower voltage rails. The measured efficiency of the conversion process is 76.9% at 30V. The power conversion process architecture is shown in a later section. This system is a second revision, which is essentially a complete redesign of the first revision taking into account the design flaws discovered during the 2012 flight. The regulators in this system are controlled by a power bus microcontroller. This device can be programed to control the power-up sequence of the regulators and can perform automatic shut-down based on user programmable criteria such as excessive current draw. Additionally, the voltage levels are programmable and can be adjusted as necessary on-the-fly. Voltage and current on each rail can be monitored independently and transmitted as part of the system telemetry if desired.



II. c. 2. FPGA CCA

Figure 2- FPGA CCA designed for the HASP 2012 flight. The dimensions are 4-in by 4-in.

The FPGA circuit card assembly serves as the system controller for the flight. Upon application of power to the payload, the Spartan-6 FPGA self-configures using an 8-bit SelectMAP Master interface to a 32-Mbit configuration memory device. The Spartan-6 FPGA contains three major hardware components: an SD card controller, a Microblaze soft processor, and the high-speed radiation sensor sampling logic. Immediately after configuration, the SD card controller performs an initialization sequence on the SD card to allow access to it via an SPI interface. The SD card is pre-loaded with the full configuration bitstream for the Virtex-6 as well as the partial bitstreams for the reconfigurable tile resources. Once the SD card initialization process is complete, control of the card is handed over to the processor. The first task of the processor is to read the configuration data from the SD card and write it to the Virtex-6 via an 8-bit SelectMAP Slave interface. Upon completion of the configuration process, the processor begins its task of sensor data collection and maintenance of the radiation tolerant computer system running on the Virtex-6. The final flight system will be designed for maximum operational autonomy with serial uplink commands available as contingencies for any possible payload failure modes.



II. c. 3. Sensor CCA

Figure 3- Radiation sensor CCA. The CCA includes the radiation sensor, sensor signal breakout board, and signal conditioning electronics.

The radiation sensor CCA consists of a custom silicon strip sensor and a chain of amplifiers used to condition the analog sensor outputs into a square pulse. The radiation sensor is a siliconbased strip detector. The substrate consists of an intrinsic silicon wafer with a P-type (Boron doped) front surface and an N-type (Phosphorous doped) rear surface. These doped regions produce an inherent electric field inside of the silicon sensor. When a radiation particle penetrates the sensor, bonds between electrons and host atoms are broken. The breaking of these bonds produces free electrons inside the substrate. The movement of these electrons effectively produces two types of charge carriers. The electrons themselves are the first carrier. The second carrier is represented by the void left by a traveling electron and is known as a hole. The combination of the traveling electrons and holes produces the desired signals. Once these carriers are generated, they are separated by the internal electric field inside the sensor. The electrons are pushed to the rear of the sensor while the holes move towards the front. These transient signals are then collected from the front and rear aluminum electrodes. The signals are input into a two-amplifier chain which amplifies and stretches the pulse for input into the high-speed sampler located in the Spartan-6. The high-speed sampler is a rising-edge triggered system which functions as a counter for each of the radiation sensor channels.

II. d. Thermal control plan

The plan for maintaining acceptable operating temperatures inside the payload will follow the demonstrated design from the 2012 flight. The approach to thermal protection seeks to maximize reflection of solar irradiation using a thin layer of aluminum and a flat, high-emissivity white paint on the external enclosure surfaces. Beneath the aluminum layer lays a half-inch of insulating foam material, which minimizes heat transfer between the enclosure and the outside environment. Within the enclosure, the heat generated by the electronics is conducted away from sensitive components through PCB ground planes, into aluminum support stand-offs located at the corner of each PCB. The heat flows through the aluminum stand-offs into a copper heatsink at the base of the electronics stack. The heatsink is placed inside the enclosure, beneath a piece of insulating foam to prevent internal radiative heat transfer. The bottom of the heatsink is in contact with the PVC mounting plate. Though not an excellent thermal conductor, it is expected that this configuration will heat the mounting plate allowing a moderate amount of heat to be radiated from the payload toward the earth. Thermal data for this design is available from 2012 HASP integration and flight. The Virtex-6 junction temperature flight data is shown below.



Figure 4- This figure shows the junction temperature of the Virtex-6 FPGA during the HASP 2012 flight. Vertical lines mark significant flight events including system shut-downs during which time no data was acquired.

II. e. Concept of Operations

The payload will be designed for autonomous flight operation with minimal administrative commands. At power-on, the system performs an initialization sequence during which the FPGAs are configured, the control processor is booted, and the data storage structures are initialized. A Microblaze soft processor is used to control the system. Its operation is interrupt-driven as it handles receipt of serial uplink commands and GPS data from the HASP platform, and transmits raw telemetry data upon query or at each expiry of fixed-interval timer. Transmitted data will include a system counter, which serves as a heartbeat to show that the system is running, radiation sensor data, available temperature data for the Virtex-6 FPGA, GPS time and position data, single event effects data, power and voltage data, and system status flags.



Figure 5- FPGA CCA architecture. This figure shows 16-Microblaze processors instantiated on the Virtex-6, the RS-232 interface to the HASP platform, and the major components of the Microblaze processor on the Spartan-6 FPGA. The flight system will likely feature a 9-Microblaze system, but the overall architecture remains unchanged.

The data will be retrieved from the HASP website as it becomes available during the flight. After retrieval, the data will be processed in MATLAB and the contents of each telemetry packet displayed on a graphical user interface. This provides the team the ability to scroll through all the received packets to determine how the system was operating. Payload commands will be available to the team during the flight. These will include commands to reset the radiation sensor counters, to reconfigure the Virtex-6, request a data transmission, or control the system voltages. The primary job of the team during the flight is to make sure the payload is transmitting data as expected and that the data values are reasonable and within appropriate operating ranges. Should data transmission cease, a power cycle will be requested to re-start the payload.

III. Team Management and Structure

The MSU team supporting this project will initially consist of three students and two faculty advisors. All of the current students are electrical engineering majors. Two of the students will

be primary team members working on the project full-time as part of ongoing research efforts. The other participant(s) will work on the project as personal schedules permit and as needed. An all-women engineering undergraduate summer program organized by Brock LaMeres typically includes the opportunity to help out with the HASP project. It is anticipated that some students from mechanical engineering will be added to the project to work on enclosure design and construction over the summer. Participants will be determined at a later time. The students are responsible for the design, development, construction, and testing of the payload. The faculty advisors carry expertise regarding the custom radiation sensor interface and operation as well as detailed knowledge of the FPGA system architecture. They take a hands-off approach to leadership, but are always available for technical consultation when needed.

The payload design and development work will be predominantly carried out by Justin Hogan and Ray Weber. These students designed the FPGA and Power CCAs respectively, and have experience working with the FPGA systems and the radiation sensors. These students will be with the team for the duration of the project. Justin and Ray will share the tasks of implementing the radiation tolerant computer architecture, developing the software necessary to control the system, testing the system and processing the data. Blaine will be available for performing sensor work to include population of sensor amplifier PCBs and packaging of radiation sensors. The summer design team will likely be tasked with building the enclosure based on design constraints determined during the 2012 project.



III. a. Team organization

Figure 6- This figure depicts the initial team structure.

III. b. Team contact information

Name	Team Role	E-mail	Phone	
Dr. Brock LaMeres	Principal Faculty Advisor	lameres@ece.montana.edu	(406) 994-5987	
Dr. Todd Kaiser	Faculty Advisor	tjkaiser@ee.montana.edu	(406) 994-7276	
Justin Hogan	Principal Team Lead	justin.hogan@msu.montana.edu	(505) 977-3844	
Ray Weber	Principal Team	raymond.weber@msu.montana.edu	(406) 994-5975	
Blaine Ferris	Member	blaineferris@gmail.com		

Table 1- This table provides the name and contact information for each team member.

III. c. Project schedule

- January to February Concurrent design work: FPGA implementation of radiationtolerant computer architecture, payload software development, and graphical user interface design.
- February Internal PDR.
- March to April Radiation sensor packaging, amplifier gain calculation and possible full-system cyclotron testing.
- April Internal CDR.
- April 19 Submit preliminary PSIP
- May to June Mechanical design work including payload enclosure design, construction, and mounting plate modification. Possible test flights using spare hardware on local sounding balloon flights.
- June 21 Submit final PSIP
- July Long-duration system bench tests, cold soak thermal testing, hot soak thermal testing if possible. General integration preparation.
- July 26 Submit FLOP
- July 29 to August 2 Integration
- August Prepare for flight operations, develop and test data processing tools.
- September 2 Flight operations

III. d. Integration and flight logistics

Team participation will be limited to one participant at HASP integration and one participant at CSBF flight operations.

IV. Payload specifications

IV. a. Weight budget

The estimated weight of the payload is 1.7-kg. Small components of unknown weight are overestimated in the weight budget based on volume and material density.

WEIGHT SUMMARY								
CIRCUIT CARD ASSEMBLY								
Part Name	Part Number	Quantity	Weight/Piece (g)	Total Weight (g)	Description Notes			
POWER CCA	U1MSUA1	1	139.7424	139.7424	Estimated weight based on POWER CCA cor	nponents		
EXPERIMENT CCA	U1MSUA2	0	0	0	No separate experiment CCA to be used on	Experiment CCA reserved for future use		
FPGA CCA	U1MSUA3	1	128.4543	128.4543	Estimated weight based on FPGA CCA comp	onents		
SENSOR_2 CCA	U1MSUA4	1	89.811	89.811	Measured weight of SENSOR CCA with radia	ation sensor		
SENSOR_1 CCA	U1MSUA5	1	89.811	89.811	Measured weight of SENSOR CCA with radia	ation sensor		
			CCA STACK TOTAL:	447.8187				
				MECHANICAL				
Part Name	Part Number	Quantity	Weight (g)	Total Weight (g)	Description	Manufacturer/Notes		
Mechanical Components	U1MSU_ENC	1	1230.134	1230.134	Includes all mounting hardware	Estimate based on material datasheets		
			MECHANICAL TOTAL:	1230.134				
	ELECTRICAL							
Part Name	Part Number	Quantity	Weight (g)	Total Weight (g)	Description	Manufacturer/Notes		
Electrical Components		1	40	40	Includes all system-level electrical hardware	2		
			ELECTRICAL TOTAL:	40				
PAYLOAD WEIGHT ESTIMATE: 1717.9								

Figure 7- This figure shows the detailed weight budget for the proposed payload.

IV. b. Mounting plate footprint

Described in later section.

IV. c. Payload height

The estimated payload height is between 5 and 6 inches. The nominal height of the electronics stack is 4 inches, and the enclosure will only as tall as necessary to accommodate this. Detailed dimensioned drawings are included in a subsequent section.

IV. d. Power budget

The estimated payload power is 7W. This corresponds to a current draw of about 220mA at 30V.

		SUPPLY VOLTAGE							
PART	REF. DES.	1.0 V6	1.0 S6	1.8	2.5	3.3	3.0	-3.0	15
Virtex-6	U14	1.139	0.213	0.000	0.105	0.000	0.000	0.000	0.000
Spartan-6		0.075	0.000	0.000	0.043	0.000	0.000	0.000	0.000
MAX3222		0.000	0.000	0.000	0.000	0.001	0.000	0.000	0.000
CP2104		0.000	0.000	0.000	0.000	0.020	0.000	0.000	0.000
XCF16P		0.000	0.000	0.010	0.010	0.005	0.000	0.000	0.000
SENSOR_1 CCA		0.000	0.000	0.000	0.000	0.000	0.380	0.180	0.000
SENSOR_2 CCA		0.000	0.000	0.000	0.000	0.000	0.380	0.180	0.000
SUPPLY CURRENT		1.214	0.213	0.010	0.158	0.026	0.760	0.360	0.000
SUPPLY POWER		1.214	0.213	0.018	0.395	0.086	2.280	1.080	0.000
LOAD POWER		5.2858							
CONVERSION EFFICIENCY		0.76							
PAYLOAD POWER		6.955							
LOAD CURRENT		0.21734375							

Figure 8- This figure shows the estimated power budget for the proposed payload.

IV. e. Telemetry

There are currently design provisions for four serial uplink commands. These commands are shown in the table below. Command values for the 'UP_ADJ_VOLT' command are still being determined. Serial uplink commands will be sent infrequently, on an as-needed basis.

MSU RTC PROPOSED UPLINK TELEMETRY FORMAT									
DACKET NAME			PACKET CONTENTS						
PACKET INAIVIE	PACKET NUIVIDER	START OF HEADING	START OF TEXT	FIRST COMMAND BYTE		2ND COMMAND BYTE	END OF TEXT	CR	LF
UP_CLR_CNTS	1	0x01	0x02	0x1	0	0	0x03	0x0D	0x0A
UP_ADJ_VOLT	2	0x01	0x02	0x2	VOLTAGE_RAIL	NEW_VOLTAGE	0x03	0x0D	0x0A
UP_RESTART	3	0x01	0x02	0x3	0	0	0x03	0x0D	0x0A
UP_RECONFIGURE	4	0x01	0x02	0x4	0	0	0x03	0x0D	0x0A

Figure 9- This figure shows the anticipated serial uplink commands.

Periodic telemetry downlink will be used for data acquisition. There are currently design provisions for five telemetry packets of varying length. These packets include system status data, time and heartbeat data, GPS data, radiation sensor data, and environmental data (power and temperature). Telemetry will consist of 1295 bytes transmitted every 20 seconds for a calculated bit rate of 518 bits per second.



Figure 10- This figure shows the anticipated telemetry packet structures.

IV. f. Analog downlink

No use of analog downlink channels is requested.

IV. g. Discrete commands

No use of discrete commands is requested.

IV. h. Payload orientation

There is no preferred location or orientation for this payload.

IV. i. Integration procedures

Integration procedures will be kept as simple as possible and the payload designed for plugand-play operation. The following steps are anticipated for a successful payload integration:

- Provide HASP managers with most recent payload documentation
- Weigh the payload to demonstrate conformance
- Apply power through HASP test bench to demonstrate current draw conformance
- Observe proper operation via RS-232 output
- Mount payload to HASP platform
- Perform power-on test to demonstrate compatibility with HASP power and telemetry systems
- Send all commands and observe proper response
- Perform environmental testing
- Spares of all electronic hardware components will be brought to integration as contingencies in the event of payload malfunction.

IV. j. Flight Procedures

No flight-line procedures will be required for this payload. After launch, the telemetry downlink will be continuously monitored by a team member to maximize scientific data quality and to ensure prompt response to any payload malfunctions.

V. Preliminary Drawings

V. a. Dimensioned mechanical drawings



Figure 11- Dimensioned mechanical drawing.

V. b. Mounting plate modifications



Figure 12- Mounting plate modifications

V. c. Power circuit diagram



Figure 13- Power conversion architecture.

V. d. Payload sketches



Figure 14- 3-D rendering of what the completed payload will look like. Includes structural support stand-offs, internal electrical connectors and electronics stack.



Figure 15- Exploded view of payload rendering.

VI. References

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