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LSU HASP Program

**Re: Monthly Status Report – June 2012**

The major design work done this month included the finalization of the power and FPGA PCB layouts and manufacturing. Both designs were completed; the power board is back from fabrication and is being tested. The FPGA board is expected to be shipped 6/29. With the PCBs out for fabrication we were able to turn our attention to the construction of the system enclosure and begin writing the software application that will run on the payload. We have been working with a team of undergraduates which is designing a weather balloon payload for a summer program here at MSU. They will be flying a mock-up of our payload which will dissipate an equivalent amount of power and will be equipped with an identical enclosure, temperature sensors, pressure sensors, 3-axis accelerometers and a MEMs gyro. To be clear, they are not flying our HASP flight hardware. As time allows, we hope to use this flight data as input into our thermal models and to test the enclosure design.

**Justin Hogan** – Finalized the FPGA PCB design, generated the CAD files, and submitted the board for manufacture. Ordered all components for the FPGA board. Worked with the undergraduate balloon team on enclosure design and construction. Began development of the payload firmware.

**Raymond Weber** – Generated CAD files for the power PCB and submitted the board for manufacture. Ordered all components for the power board. Populated and began testing of the power board. Worked with the undergraduate balloon team on sensor requirements and power supply design.

**Adrien Lambert** – Continued work on payload enclosure thermal design and worked with the undergraduate balloon team on construction of the enclosure.

**Blaine Ferris** – Continued thermal analysis work on the system electronics stack using HyperLynx Thermal.

**Issues encountered during payload design and development**

- The FPGA board is a 12-layer PCB with very small clearance and trace requirements. This resulted in an 11-day fabrication lead time, which slipped several days on the manufacturer's end. We're able to work in parallel while the board is out, but the schedule is getting tight.

## Milestones Achieved

- Power PCB fabricated, populated, and undergoing testing
- FPGA PCB submitted for fabrication

## Current team members and leaders

Name	Team Role	E-mail	Phone
Dr. Brock LaMeres	Principal Faculty Advisor	lameres@ece.montana.edu	(406) 994-5987
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Adrien Lambert	Team Member	adrien.lambert@msu.montana.edu	
Blaine Ferris	Team Member	blaine.ferris@gmail.com	



Figure 1: Power CCA during assembly and test.

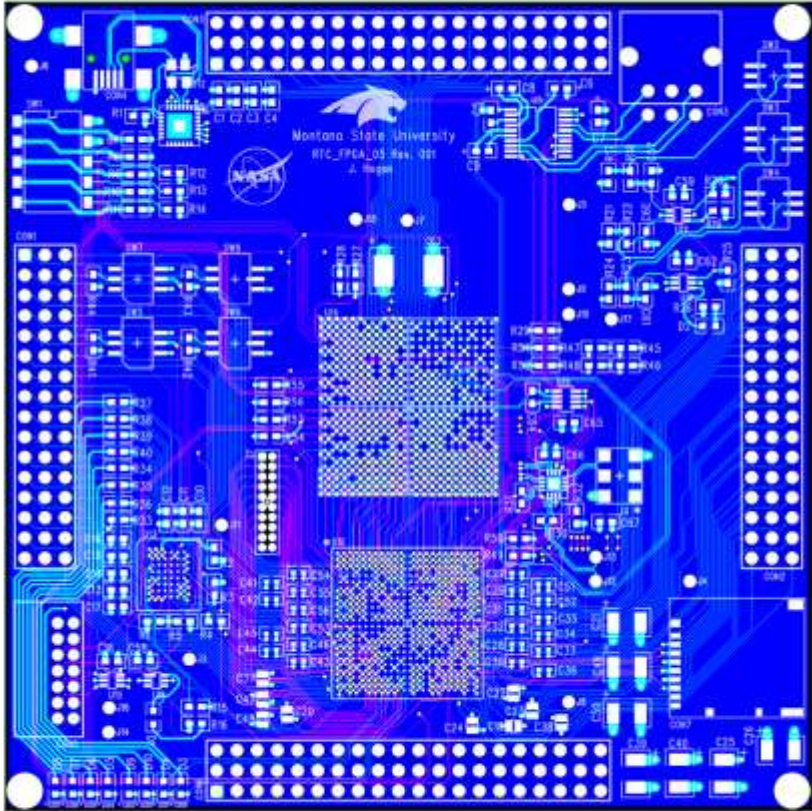


Figure 2: FPGA PCB rendering with all layers visible.