



HASP Student Payload Application for 2012

Payload Title: Single Event Effect Detector		
Payload Class: (check one) <input checked="" type="checkbox"/> Small <input type="checkbox"/> Large	Institution: Montana State University	Submit Date: 12/16/2012
Project Abstract <p>As part of MSU's research effort into building radiation tolerant computing systems for aerospace applications, a radiation sensor has been developed to provide environmental awareness to the flight computer. This sensor is designed to detect the spatial location of radiation strikes with energy levels that cause single event effects in modern CMOS electronics. These are typically due to trapped protons and heavy ions. Our HASP payload consists of a radiation sensor system in addition to an FPGA-based flight computer that will record strikes throughout the duration of the flight.</p>		
Team Name: MSU Radiation Tolerant Computing (MSU RTC) Group		Team or Project Website:
Student Team Leader Contact Information:		Faculty Advisor Contact Information:
Name:	Justin Hogan	Dr. Brock J. LaMeres
Department:	Electrical and Computer Engineering	Electrical and Computer Engineering
Mailing Address:	540 Cobleigh Hall	533 Cobleigh Hall
City, State, Zip code:	Bozeman, Montana, 59717	Bozeman, Montana, 59717
e-mail:	justin.hogan@msu.montana.edu	lameres@ece.montana.edu
Office telephone:		(406) 994-5987
Cell:	(505) 977-3844	
FAX:	(406) 994-5958	(406) 994-5958

I. Payload Description

An ongoing research project being conducted by MSU's Radiation Tolerant Computing group is the design and development of a radiation-tolerant space flight computer architecture. In space, electrical systems are not afforded the protection of Earth's atmosphere or magnetosphere against interactions with high-energy particles such as heavy ions, protons, electrons, cosmic rays, etc. When impacted by these particles energy may be transferred to sensitive regions of the circuit resulting in deposition of parasitic charge, induction of electrical currents, or physical damage to the constituent crystal lattice structure of the device substrate material. These events may result in the changing of a transistor threshold voltage to the point that it may be impossible to turn the transistor on or off, unanticipated clocking of data through a system, or uncontrolled and undetectable changes in device memory bit values. Radiation tolerance refers to a system's ability to continue operating nominally after such an event with minimal interruption.

Radiation tolerance is implemented in many ways. Circuits can be designed using specialized fabrication processes to minimize the radiation cross-section, or the area of the integrated circuit that is susceptible to radiation. These parts are typically more expensive and perform slower than their non-hardened counterparts. Heavy shielding may be used to protect critical systems. This option is non-ideal due to the high cost of putting materials into orbit, and shielding material may add substantial weight to a payload. Another way to protect systems from radiation faults is by incorporating circuitry in triplicate and routing redundant signals to a majority-rules voting sub-circuit. In this way, radiation strikes are detected by non-uniform inputs at the voter, and the fault is prevented by only passing the majority signal. The probability of two regions being simultaneously faulted in the same way is low and tolerance is gained through the use of redundant circuitry.

The system proposed herein leverages the flexibility of field programmable gate arrays (FPGAs) to implement triple-modulo redundancy (TMR), FPGA configuration SRAM readback scrubbing, partial reconfiguration, and custom radiation sensors to achieve radiation tolerance. In FPGAs, designs can implement triple-modulo redundancy (TMR) architecture without the costs of added hardware. This design will feature 16 reconfigurable Microblaze microprocessors instantiated on partial reconfiguration tiles within an FPGA. Three of these tiles will be active at a given time with the remaining 13 processors reserved as spares. The microcontroller outputs will be sent to a second FPGA which houses the voter circuitry portion of the TMR architecture. If one of the three active processors is found by the voter to have invalid outputs, the tile will be deactivated and a spare will be activated in its place. The deactivated (faulted) tile is then reconfigured by the control FPGA and made available to the system as a spare. As the processor tiles execute their application code, the control FPGA continually reads the configuration SRAM of the main FPGA and checks it against a master configuration bitstream. The configuration bitstream defines the behavior of the FPGA. This memory is susceptible to radiation effects and changes to its contents change the behavior of the device. As when the voter identifies faults in

the main FPGA, the readback scrubber system can identify configuration faults in the FPGA and repair them using the same partial reconfiguration technique.

The system under development at MSU builds on a traditional TMR/scrubber/partial reconfiguration (PR) architecture with the addition of a custom silicon radiation sensor capable of detecting radiation strikes. The radiation sensor is a silicon based strip detector. The substrate consists of an intrinsic silicon wafer with a P-type (Boron doped) front surface and an N-type (Phosphorous doped) rear surface. These doped regions produce an inherent electric field inside of the silicon sensor. When a heavy radiation particle penetrates the sensor, bonds between electrons and host atoms are broken. The breaking of these bonds produces free electrons inside the substrate. The movement of these electrons effectively produces two types of charge carriers. The electrons themselves are the first carrier. The second carrier is represented by the void left by a traveling electron and is known as a hole. The combination of the traveling electrons and holes produces the desired signals. Once these carriers are generated, they are separated by the internal electric field inside the sensor. The electrons are pushed to the rear of the sensor while the holes move towards the front. These transient signals are then collected from the front and rear aluminum electrodes. The front and rear of the sensor consist of 16 parallel electrodes. The rear electrodes are rotated 90 degrees with respect to the front side. This produces 256 unique locations that can be sensed by the radiation sensor. The signals coming out of the sensor are then input into an electronics board that shapes and amplifies these signals so that they can be used by a computer system. Figure 1 below shows a picture of the radiation sensor proposed for flight.



Figure 1: This figure depicts the radiation sensor and package board proposed for flight. The board dimensions are ~50mm x ~60mm.

The proposed payload will continue the testing process associated with the development of any new technology by demonstrating the functionality of the radiation sensor when subjected to ionizing radiation in Earth's upper atmosphere. Previously, this sensor has been flown on a payload designed under the High Altitude Balloon Payload Design Program in collaboration with NASA and the Montana Space Grant Consortium (MSGC). In this flight, the radiation sensor and control electronics logged radiation strikes in an ascent to nearly 100,000 feet MSL. Before termination, the data showed a strong exponential trend in the number of radiation strikes per

minute increasing from zero to 20 as the payload passed through the stratosphere (Fig. 2). A similar payload featuring a two-sensor stack-up is proposed for participation in the 2012 HASP flight.

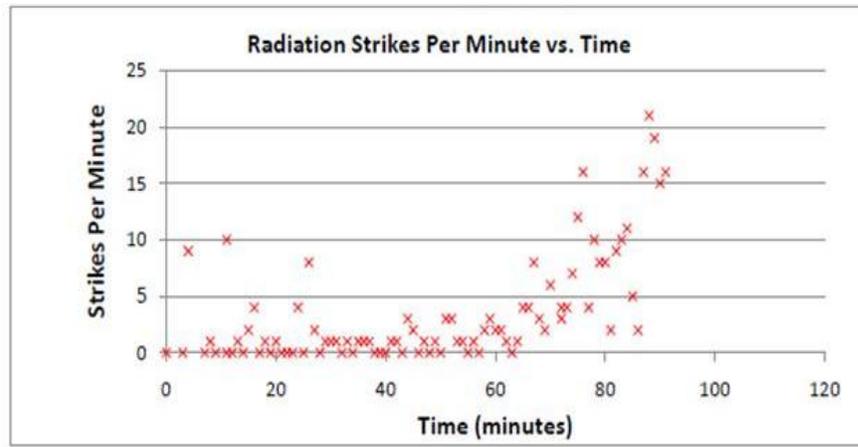


Figure 2: Detected radiation strikes using custom silicon radiation sensor on BOREALIS balloon flight payload. At time 60-minutes the payload was at approximately 70,000-ft. MSL. (http://www.coe.montana.edu/ee/lameres/project_summer11_payload_design.htm)

I. a. Scientific Objectives

The objective of our mission is to measure the performance of our custom single event effect sensor in a high-altitude environment. The strike rate profile generated by the radiation sensor will allow performance comparison with data acquired by independent payload systems on separate flights with similar flight profiles. These data will allow relative sensor sensitivity comparisons and provide feedback regarding the performance of the custom design. By also feeding the radiation sensor outputs into the fault repair and recovery system on the FPGA several performance parameters can be validated. Each sensor in the two-sensor stack provides the spatial location for a radiation strike. This information can be used to extract a radiation trajectory estimate. Radiation trajectory information can be compared with the corresponding location of an observed FPGA fault, should it occur, and the accuracy of the trajectory estimate can be assessed. With this flight it is anticipated that the radiation-tolerant computer system will demonstrate real-time fault detection and recovery and correlate said faults to observed radiation sensor strike data.

I. b. High-level review of payload systems

The payload system will be a circuit card assembly (CCA) stack consisting of the following:

- Power CCA
- Experiment CCA (optional)
- FPGA CCA

- Lower radiation sensor CCA
- Upper radiation sensor CCA

The power CCA will accept as input the 28-33V power supply voltage provided by the HASP system and down-convert it to the required payload voltages. The required voltages are those that power the FPGA CCA and the two radiation sensor CCAs. Where possible the power CCA will use high-efficiency switching power converters to produce required voltage levels.

The experiment CCA is incorporated as part of a re-usable stack architecture in which the radiation-tolerant FPGA system can interface with project-specific circuitry on the experiment board. The experiment CCA will not be populated for this project.

The FPGA CCA is the primary payload system. This board will feature two FPGA chips: one “main” FPGA that is available as a general purpose computing system, and one “control” FPGA responsible for payload control, collecting data from the radiation sensors, scrubbing the configuration memory of the main FPGA, voting on TMR outputs from the main FPGA and performing partial reconfiguration on faulted regions. Additionally, the control FPGA is responsible for configuring the main FPGA during system start-up.

The payload will have two sensor CCAs in the stack each one populated with a radiation sensor as described previously. These sensors are one of three ways the system can detect and respond to radiation strikes and their effects. When ionizing radiation passes through the sensor the signal is amplified and passed to the control FPGA board through stack connectors. The control FPGA interprets the inputs and determines the spatial location of the strike on each sensor. Using this information, the configuration memory scrubbing circuit is directed to the location most likely affected by the radiation strike. If faults are found in the configuration memory, the affected tile is partially reconfigured. The other ways of detecting radiation effects come through the normal operation of the voter circuitry and the continual operation of the configuration memory readback scrubber system.

I. c. Statement of principle of operation

The system will be designed for single-mode autonomous operation for the duration of the flight. At power-on, the control FPGA will perform an initialization sequence and begin monitoring the radiation sensors for strikes. During this sequence, the control FPGA self-configures then configures the main FPGA. A configuration SRAM scrubbing circuit on the control FPGA will continually check the main FPGA through its configuration interface for faulted partially reconfigurable tiles. As radiation strikes are detected, either by the voter, the readback scrubber, or the radiation sensors, the location of the strike, the cumulative number of strikes and a timestamp will be stored locally. For each detected strike, the SRAM scrubber will check the FPGA areas that were most likely affected, and indicate whether a fault was induced. In this way, the number of faults versus the number of detected strikes can be studied. It is also conceivable that the FPGA may be faulted by radiation from incidence angles large enough to

bypass the radiation sensors. As they occur, these FPGA faults and locations will also be stored locally. The system will be programmed to transmit summary data regarding the number of strikes for each location as well as overall system information. Details of the telemetry and command structure are discussed in a later section.

I. d. Thermal Control Plan

As the payload will be operated in extreme temperature environments over the course of a flight, considerations for cooling or heating the payload are critical to mission success. The most sensitive components to heating and cooling cycles will be the system FPGAs. To help minimize the amount of radiative solar heating the payload's outer enclosure will be of a light, reflective color. A layer of insulation will be added to the enclosure to help keep the system warm in very cold temperatures. Preliminary thermal analysis to determine internal payload temperature was performed for an ascent temperature profile using data from a previous launch (Figure 3). This analysis assumed the payload was dissipating the maximum allowed power of ~15W as heat, which was found to be very conservative following payload power analysis. The analysis shows the internal temperature approaching 80°C as the payload reaches 120,000-feet. We have included provisions in our weight budget for adding heat sink components to the FPGAs, including routing to a high thermal conductivity heat dissipation plate on the bottom side of the payload system. As available, industrial-rated circuit components are being selected for use, providing a -25°C to 85°C operating region. Further thermal analysis is ongoing to determine payload temperature during hot and cold soaks that may be encountered during the float portion of the flight to gain confidence that our thermal management solution will allow systems to operate within thermal limits at all times. As refined power dissipation estimates are available the thermal analyses will be re-run.

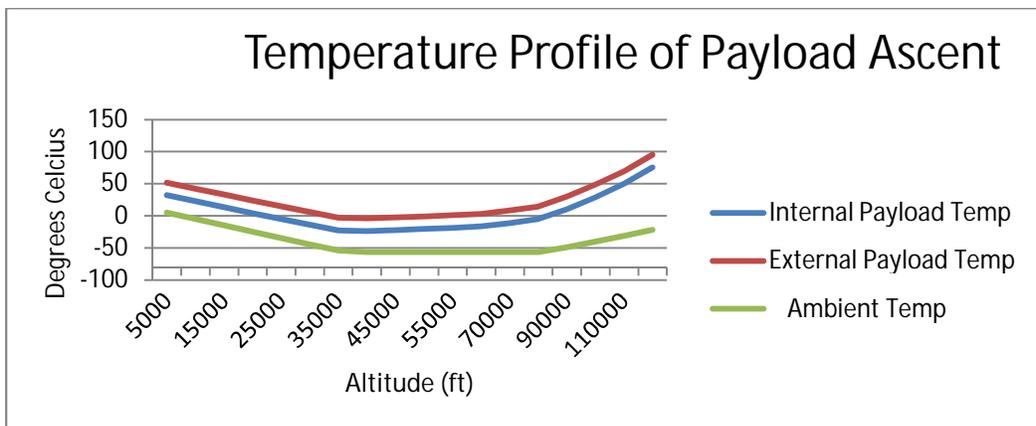


Figure 3: Simulated temperature profiles during ascent assuming worst-case power dissipation of 15W. Temperatures remain within operating constraints, but suggest need for heat sink design to dissipate heat from the payload. Component heat sinks with plate for radiative cooling of the payload are being considered.

II. Team Management and Structure

The MSU RTC team supporting this project will consist of five students and two faculty advisors. Of the students, four are electrical engineering graduate students and one is a mechanical engineering graduate student. Two of the students will be primary team members, and the remaining three will act as secondary support members as they will be graduating in spring 2012. The faculty advisors carry expertise regarding the custom radiation sensor interface and operation as well as detailed knowledge of the FPGA system architecture. The organization chart of Figure 4 shows this team hierarchy graphically. Table 1 provides the names and contact information for the team members.

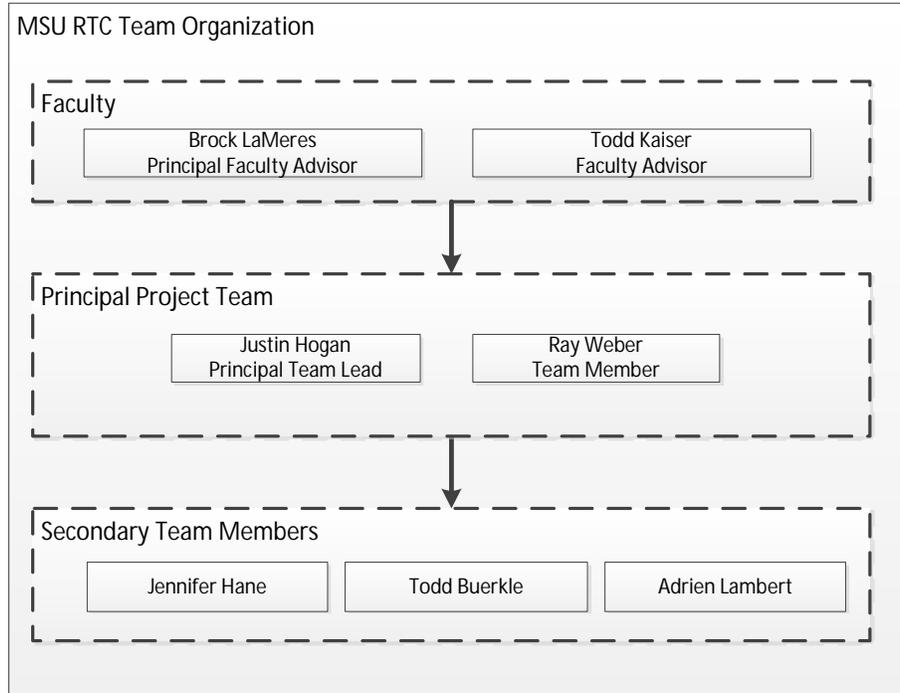


Figure 4: Team Organization Chart

Name	Team Role	E-mail	Phone
Dr. Brock LaMeres	Principal Faculty Advisor	lameres@ece.montana.edu	(406) 994-5987
Dr. Todd Kaiser	Faculty Advisor	tjkaiser@ee.montana.edu	(406) 994-7276
Justin Hogan	Principal Team Lead	justin.hogan@msu.montana.edu	(505) 977-3844
Ray Weber	Principal Team	raymond.weber@msu.montana.edu	(406) 994-5975
Jennifer Hane	Team Member	jennifer.hane@msu.montana.edu	
Todd Buerkle	Team Member	toddbuerkle@gmail.com	
Adrien Lambert	Team Member	adrien.lambert@msu.montana.edu	
Elizabeth Clem	Team Member	lizi.clem@gmail.com	

Table 1: Team Contact Information

II. a. Team Effort Organization

The payload design and development work will be predominantly carried out by Justin Hogan and Ray Weber. Both PhD students, these students have experience working with the FPGA systems and the radiation sensors and will be with the team for the duration of the project. Justin Hogan will be responsible for the design of the FPGA board, experiment board, and power conversion board as well as maintaining awareness of the overall project requirements including interface specifications, physical system constraints, project deadlines, etc. Ray Weber will assist with porting the existing FPGA system design to the new hardware platform, maintain a working knowledge of all payload systems, and help with interface testing and system firmware development as necessary.

Jennifer Hane has extensive working knowledge of the radiation-tolerant FPGA system architecture and will serve as a consultant as the current FPGA design is ported to the new HASP payload hardware. Jennifer will be instrumental in conveying knowledge regarding the reconfigurable architecture, including the configuration SRAM scrubbing logic, the partial reconfiguration processes, TMR system design and other aspects of the FPGA board design. Jennifer has been involved with previous MSU HASP payloads, so she is also able to provide relevant design input based on her experience.

Todd Buerkle designed and has intimate knowledge of the radiation sensor board. He manufactured the generation of sensors that will be in the payload using MSU's in-house micro-fabrication facilities. His research involves testing the radiation sensors and amplification circuitry in an ion beam at a cyclotron and the work he performs in that capacity is directly supportive of our sensor requirements for the HASP payload.

Adrien Lambert will be available to help with the mechanical design aspects of payload development. This includes maintaining system drawings, consulting on payload mounting considerations to ensure a robust design, and assisting with vibration and thermal testing as necessary. Adrien has previous ballooning experience as he worked with the MSU team that flew the radiation sensors as part of the previously mentioned MSGC program.

II. b. Project Timeline

The following milestones are crucial to having a payload ready for thermal/vacuum testing in May 2012, payload integration on July 30, 2012, and flight as early as August 31, 2012:

- Power conversion, experiment, and FPGA CCA requirements review – January 13
- Power conversion, experiment, and FPGA CCA design review – February 17
- Power conversion, experiment, and FPGA CCA testing – March 1
- Complete CCA stack testing – March 15
- Mounting and enclosure system complete – April 1
- Radiation-tolerant FPGA architecture hardware port – April 15

- System Firmware complete – April 15
- Thermal/Vac – May 1 (TBD)
- Follow-on testing – May – July 30
- Student payload integration – July 30-August 3
- Flight prep and operations – August 26 – August 31

II. c. Team Operations at CSBF

Team operations at CSBF will include two student team members and one faculty advisor at most.

III. Payload Specifications

III. a. Mechanical

III. a. i. Anticipated Use of HASP Resources

The estimated weight of the payload is being tracked through a detailed set of linked spreadsheets that itemizes the components on each CCA, the mounting hardware for securing the CCA stack, the mounting hardware for securing the enclosure to the HASP structure, enclosure materials, electrical connectors and thermal control components. In general it is difficult to obtain actual weights for many of the small circuit components to be used on the individual circuit cards. In cases where the weight of a component was unknown a gross overestimation was made by substituting the weight of a much more massive component. Components with estimated weight values were marked and tracked in the spreadsheets for updating with actual weight measurements as they become available. The current payload weight summary is presented in the figure below. The estimated payload total weight is 1.622-kg. This estimate includes all major system components. Uncertainties are primarily in the number and individual weights of miniscule surface-mount resistors, capacitors, and inductors. However, weight estimates are provided with overestimates of the required quantities. Additionally, excess weight was included to allow design flexibility regarding inclusion of an external heat sink.

MSU RTC PAYLOAD_04 WEIGHT SUMMARY						
CIRCUIT CARD ASSEMBLY						
Part Name	Part Number	Quantity	Weight/Piece (g)	Total Weight (g)	Description	Notes
POWER CCA	U1MSUA1	1	139.7424	139.7424	Estimated weight based on POWER CCA components	
EXPERIMENT CCA	U1MSUA2	0	0	0	No separate experiment CCA to be used on: Experiment CCA reserved for future use	
FPGA CCA	U1MSUA3	1	128.1149	128.1149	Estimated weight based on FPGA CCA components	
SENSOR_2 CCA	U1MSUA4	1	89.811	89.811	Measured weight of SENSOR CCA with radiation sensor	
SENSOR_1 CCA	U1MSUA5	1	89.811	89.811	Measured weight of SENSOR CCA with radiation sensor	
CCA STACK TOTAL:				447.4793		
MECHANICAL						
Part Name	Part Number	Quantity	Weight (g)	Total Weight (g)	Description	Manufacturer/Notes
Mechanical Component	U1MSU_ENC	1	1135.41	1135.41	Includes all mounting hardware	
MECHANICAL TOTAL:				1135.41		
ELECTRICAL						
Part Name	Part Number	Quantity	Weight (g)	Total Weight (g)	Description	Manufacturer/Notes
Electrical Components		1	40	40	Includes all system-level electrical hardware	
ELECTRICAL TOTAL:				40		
PAYLOAD WEIGHT ESTIMATE:				1622.8893		

Figure 5: This figure presents the estimated weight budget for the payload CCA stack, mounting hardware, enclosure, and electrical connectors. Component weights were included as available in datasheets, and gross overestimates were used in cases where product weights were unavailable. The weight estimates for each subsystem were taken from linked spreadsheets containing itemized weights for constituent parts.

It is anticipated that the payload will make use of the entire mounting plate footprint area, but easily remain within the specified 5.875-in. by 5.875-in. constraints. The payload electronics are limited in footprint size by the dimensions of the circuit board stack which is 4-in. by 4-in. The stack will be centered in the mounting area. The area around the stack will be used for affixing a protective enclosure through which the power and communication signals will be passed to the payload.

Again, the payload footprint will be 4-in. by 4-in. with an enclosure occupying the remainder of the available mounting area. A conservative estimate of the maximum height of the circuit board stack is 5-in. which is significantly less than the ~12-in. allowed for small payloads. The enclosure will add to this height, but the overall payload size will easily remain within specifications.

The only orientation requirement for this payload is that it be mounted on the HASP structure such that the radiation sensors are facing upward (toward the balloon). There are no specific locations on the fixture that would be more or less advantageous for this payload, so there is flexibility in where it is placed. There is a request for a single discrete signal in the electrical subsection below. Payload positions 1, 2, and 5 would accommodate this request. However, this is not a stringent requirement and this payload can yield to others with more strict needs for extra discretely in which case payload positions 3,4,6,7 and 8 would be fine.

III. b. Electrical

The power consumption for the payload will be determined by three main system components: the efficiency of the power conversion process, the speed of operation of the FPGA system and the radiation strike rate. The power consumed by the FPGAs in the system depends on the logic resource utilization of the devices, clock rates, etc. so our power estimates will change as our FPGA designs iterate. The power estimates below are based upon our most

recently synthesized FPGA designs. As power requirements become clearer, options exist for minimizing power consumption by choosing lower speed-grade FPGA components and utilizing lower I/O voltage levels. Preliminary power dissipation estimate for the proposed payload is ~7.7W (0.24A @ 32V). This incorporates an expected overall power supply efficiency of around 70%. This power supply document will be maintained as devices are added to or removed from the design.

	SUPPLY VOLTAGE							
	1.0	1.2	1.8	2.5	3.0	-3.0	3.3	15
Virtex-6	1.139	0.213	0.000	0.105	0.000	0.000	0.000	0.000
Spartan-6	0.075	0.000	0.000	0.043	0.000	0.000	0.000	0.000
MAX3222	0.000	0.000	0.000	0.000	0.000	0.000	0.001	0.000
CP2104	0.000	0.000	0.000	0.000	0.000	0.000	0.020	0.000
XCF16P	0.000	0.000	0.010	0.010	0.000	0.000	0.005	0.000
SENSOR_1 CCA	0.000	0.000	0.000	0.000	0.380	0.180	0.000	0.000
SENSOR_2 CCA	0.000	0.000	0.000	0.000	0.380	0.180	0.000	0.000
SUPPLY CURRENT	1.214	0.213	0.010	0.158	0.760	0.360	0.026	0.000
SUPPLY POWER	1.214	0.256	0.018	0.395	2.280	1.080	0.086	0.000
LOAD POWER	5.3284							
CONVERSION EFFICIENCY	0.7							
PAYLOAD POWER	7.612							
LOAD CURRENT	0.237875							

Figure 6: Preliminary payload power estimates. Each row represents the current drawn by the specified device at the voltage level in each column. The totals for each supply are summed across the bottom and the total power calculated.

Downlink telemetry will be used to transmit summary data and system status messages at regular intervals. The maximum estimated number of bytes sent in a single telemetry downlink session is 930. A bit rate of 1200-bps will allow these telemetry packets to be transmitted to the HASP system in 6-7 seconds. It is currently anticipated that telemetry sessions will occur once per minute, and queried data packets will be transmitted as requested through serial uplink commands. The mission critical data will include radiation strike count and sensor locations, observed FPGA fault numbers and locations, associated timestamps, and the most recently received uplink command. Figure 7 shows the preliminary list of telemetry packets along with a description of the packet structure.

MSU RTC PAYLOAD_04 TELEMETRY FORMAT													
PACKET NAME	PACKET NUMBER	PACKET CONTENTS											
		B0	B1	B2:B5	B6:B9	B10:B11	B12	B13	B14	B15	B16	B17:755	
TLM_NUM_STRIKES	01		0x01	-- -- -- --	-- -- -- --	0x03	0x00	--	CUMULATIVE STRIKE COUNTS PER TILE				
TLM_STRIKE_INFO	02		0x02	-- -- -- --	-- -- -- --	0x00	0x02	--	SEN1_X:SEN1_Y	SEN2_X:SEN2_Y			
TLM_ACTIVE	03		0x03	-- -- -- --	-- -- -- --	0x00	0x02	--	ACTIVE_0:ACTIVE_1	ACTIVE_2:NULL			
TLM_SCRUB_FAULTS	04		0x04	-- -- -- --	-- -- -- --	0x00	0x04	--	SCRUB_CNT	SCRUB_CNT	SCRUB_CNT	SCRUB_CNT	
TLM_VOTE_FAULTS	05		0x05	-- -- -- --	-- -- -- --	0x00	0x04	--	VOTER_CNT	VOTER_CNT	VOTER_CNT	VOTER_CNT	
TLM_TEMP	06		0x06	-- -- -- --	-- -- -- --	0x00	0x02	--	CTRL_JUNC_TEMP	MAIN_JUNC_TEMP			
TLM_VOLT	07		0x07	-- -- -- --	-- -- -- --			--					
TLM_ECHO	08		0x08	-- -- -- --	-- -- -- --	0x00	0x01	--	ACKD_CMD_NUM				
TLM_CTRL_START	09		0x09	-- -- -- --	-- -- -- --			--					
TLM_MAIN_START	10		0x0A	-- -- -- --	-- -- -- --			--					
TLM_SHTDN	11		0x0B	-- -- -- --	-- -- -- --	0x00	0x01	--	SHTDN_CODE				

BYTE NUMBER	BYTE NAME	BYTE DESCRIPTION
B0	SYNC BYTE PATTERN	Unique bit pattern unlikely to occur in data to signify beginning of telemetry packet
B1	PACKET TYPE INDICATOR	Packet type identifier
B2	TIME STAMP(0:7)	Macro time stamp (seconds since 01 JAN 1970)
B3	TIME STAMP(8:15)	Macro time stamp (seconds since 01 JAN 1970)
B4	TIME STAMP(16:23)	Macro time stamp (seconds since 01 JAN 1970)
B5	TIME STAMP(24:31)	Macro time stamp (seconds since 01 JAN 1970)
B6	TIME STAMP(0:7)	Micro time stamp (nanoseconds since last second)
B7	TIME STAMP(8:15)	Micro time stamp (nanoseconds since last second)
B8	TIME STAMP(16:23)	Micro time stamp (nanoseconds since last second)
B9	TIME STAMP(24:31)	Micro time stamp (nanoseconds since last second)
B10	RECORD SIZE(15:8)	Number of data bytes contained in the data packet (1 to 65536)
B11	RECORD SIZE(7:0)	Number of data bytes contained in the data packet (1 to 65536)
B12	CHECKSUM	Least significant byte of record checksum
B13:B(RECORD SIZE)	PACKET DATA	Packet data contents

Figure 7: This figure shows a preliminary list of telemetry packets used by the payload. It depicts the packet structure including synchronization pattern, packet header, checksum and data contents.

The use of uplink commands will be for the purpose of querying system status, triggering system resets, reconfiguring the main FPGA, etc. As the system will be operating single-mode commands will only be sent when data in the telemetry suggests that a reset or reconfiguration of the system is needed. As such, no specific time or ordering of command issuance can reasonably be anticipated. Upon receipt of a command the payload will decode the contents and echo the command in the downlink telemetry stream for verification purposes. Each command will have an associated response that will be present in the telemetry stream which can also be used to verify the command was executed by the payload. Figure 8 provides a list of anticipated commands along with command structure and contents. A checksum will be computed for each packet and filled-in as available.

MSU RTC PAYLOAD_04 COMMAND FORMAT												
COMMAND NAME	COMMAND NUMBER	COMMAND CONTENTS								PACKET	CHECKSUM	BITS
		B1	B2	B3	B4	B5	B6	B7				
CMD_CTRL_RST	01	0x01	0x02	0x4-	0x01	0x03	0x0D	0x0A	01024-01030D0A		56	
CMD_CTRL_CFG	02	0x01	0x02	0x4-	0x02	0x03	0x0D	0x0A	01024-02030D0A		56	
CMD_MAIN_CFG	03	0x01	0x02	0x4-	0x03	0x03	0x0D	0x0A	01024-03030D0A		56	
CMD_STRIKES	04	0x01	0x02	0x4-	0x04	0x03	0x0D	0x0A	01024-04030D0A		56	
CMD_SCRUB_FAULTS	05	0x01	0x02	0x4-	0x05	0x03	0x0D	0x0A	01024-05030D0A		56	
CMD_VOTE_FAULTS	06	0x01	0x02	0x4-	0x06	0x03	0x0D	0x0A	01024-06030D0A		56	
CMD_ACTIVE	07	0x01	0x02	0x4-	0x07	0x03	0x0D	0x0A	01024-07030D0A		56	
CMD_HEALTH	08	0x01	0x02	0x4-	0x08	0x03	0x0D	0x0A	01024-08030D0A		56	
CMD_SHTDN	09	0x01	0x02	0x4-	0x09	0x03	0x0D	0x0A	01024-09030D0A		56	
CMD_TILE_MUTE	10	0x01	0x02	0x4-	0x--	0x03	0x0D	0x0A	01024--030D0A		56	

Figure 8: This figure shows a preliminary uplink command list for the payload. More detailed descriptions of the commands and conditions under which they will be sent is also maintained.

There is no presently anticipated use of the analog downlink resources.

In addition to the power-on and power-off discrete signals, a single discrete signal for power-on reset of the FPGA system is requested.

III. c. Procedural, Integration and Operations

As part of payload design, test procedures will be developed to ensure reliability of the serial communications interface. It is feasible to emulate the HASP Mini-SIP communication system and exercise the payload interface signals using an 8-N-1, 1200 baud RS-232 connection, including the TX and RX buffering done by the HASP system. All uplink system commands can be sent to the payload and the payload response can be evaluated. Additionally, the power provided to the payload during bench testing can be varied to simulate the initial ~32-V and final ~28-V power supply voltage fluctuations.

Using the HASP Payload Integration Certification as a guideline, these lab test procedures will naturally flow into a set of integration procedures for use during HASP system integration. It is anticipated that as part of the integration process the system will be powered by the HASP power system. As such, a detailed schematic of the power wiring and conversion system will be provided. The following major steps are anticipated during integration:

- Weigh the payload to ensure weight compliance
- Perform continuity test on power connector to verify proper pin assignment
- Apply system voltage and measure current draw
- Inspect interior of payload enclosure for structural integrity, insulation adequacy.
- Verify CCA stack mount integrity and stability on mounting plate
- Affix enclosure and verify secure attachment
- Perform thermal test including cold and hot soaks
- Monitor system outputs to ensure proper operation during environmental tests
- Depressurize atmosphere to demonstrate proper operation in low-pressure environment. Demonstrate thermal control in absence of convective cooling
- Transmit each telemetry packet to HASP system, verify packet integrity
- Verify 1200-bps bit rate
- Parse downlink data from HASP website to ensure proper transmission, storage, and recovery
- Send all 10 uplink commands to payload and verify proper response
- Submit and review flight operations procedures

The payload will be designed for single-mode operation from start to finish with system initialization occurring automatically with application of HASP system power. In general, no complex interactions with the system will be required as the payload will remain in a single mode of operation throughout the entire flight. Team members will be on-hand as needed during preparation for flight to address any last-minute concerns with the payload. The team will also

have a representative present with mission control personnel to monitor the status of the payload, the downlink telemetry data, and to request any necessary uplink commands verbally as described in the CFP. Preliminary flight operations procedures include:

- Install payload on HASP structure
- Apply system power
- Verify receipt of start-up telemetry (TLM_CTRL_START, TLM_MAIN_START)
- If improper power-up, command reset (CMD_CTRL_RST)
- If proper start-up, continue monitoring telemetry data for signs of proper operation (increasing strike counts, changing strike locations, changing FPGA core voltages and junction temperatures, changing timestamps in telemetry packets, etc.)
- If a sensor strip is suspected faulty (anomalously quantity and frequency of strikes) send a channel mute command to stop monitoring the channel (CMD_TILE_MUTE)
- If improper operation of main FPGA is suspected send a reconfiguration command (CMD_MAIN_CFG)
- If improper control operation is suspected send control reset command (CMD_CTRL_RST)
- Continuously monitor telemetry stream, interpret data, and be available for command requests
- Send command to shut down the system at end of flight (CMD_SHTDN)

IV. Preliminary Drawings

IV. a. HASP Interface and Power Conversion

HASP interface will consist of termination of the EDAC and DB9 connectors on the mounting plate with appropriate connectors on the power CCA and FPGA CCA respectively. The current design choice is to forego a bulkhead connector in favor of passing wiring directly through an aperture on the side or bottom of the enclosure and sealing the aperture to prevent debris from entering the system. Power conversion parts selection has largely been completed with the exception of +3V and -3V rails, which will be similar to those selected for the 2.5V and 3.3V supplies. The Figure 9 shows preliminary interface architecture with power conversion and efficiency as available.

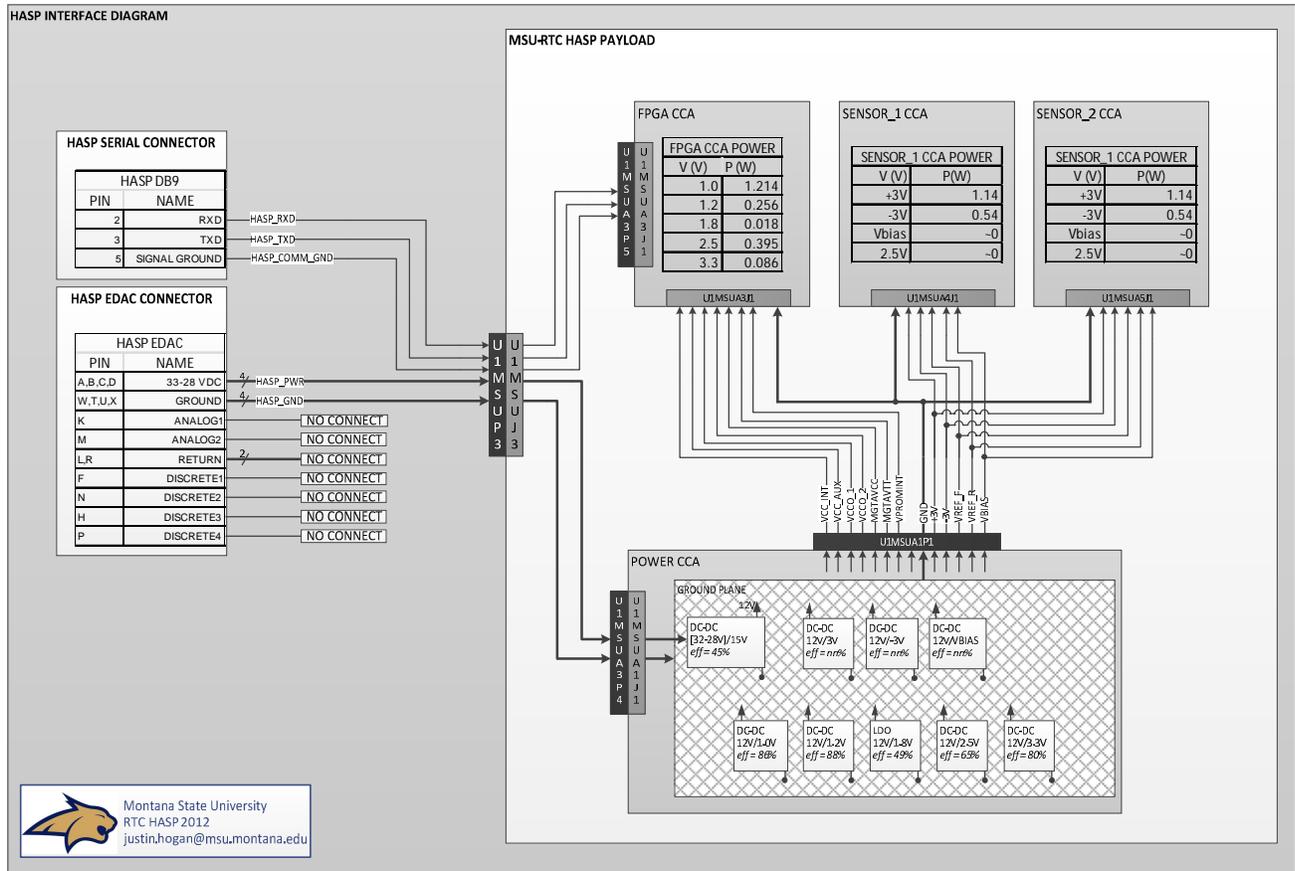
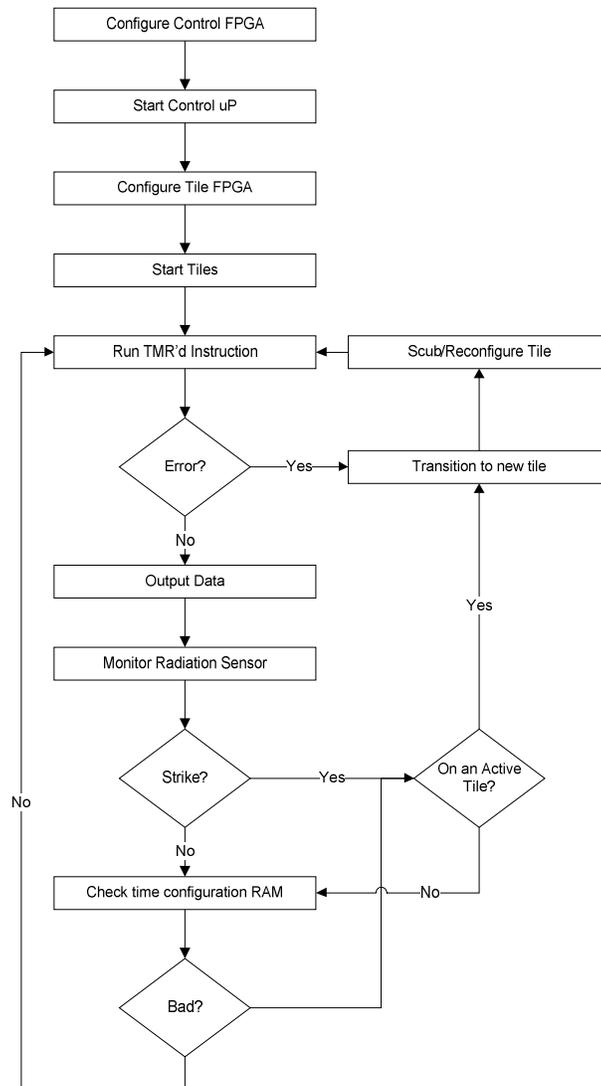


Figure 9: This figure shows a preliminary HASP interface architecture with power conversion and delivery interconnects.

IV. b. Preliminary software flow diagram

The following flow chart shows the preliminary system software operation during flight. Upon system start-up, the control FPGA will self-configure and begin executing a system control application. The first task of the microprocessor on the control FPGA is to configure the main FPGA. After configuration of the main, the active tiles are enabled and the microprocessors on each tile begin executing an application. The application executed by the active tiles is not important to system operation and may be as simple as a counter that produces outputs for comparison by the TMR voter circuitry. Each tile executes a TMR'd instruction and passes its outputs to the voter. If the outputs are valid they are allowed to pass. If outputs are invalid the active tile is faulted and a new tile is brought online in its place. The faulted tile is scrubbed and reintroduced as a spare tile. The radiation sensor is monitored for strikes, the location decoded, and if it is determined to have impacted an active tile the tile is faulted and the system brings on a replacement. There are always three active tiles in running on the main FPGA. Provisions for transmitting telemetry data at the specified intervals and for processing received uplink commands will be incorporated as this flow chart is refined.



IV. c. Mounting Plate Modifications

Four holes will be drilled in the mounting plate to align with the mounting holes on the CCAs in the stack. The payload electronics stack will be affixed to the mounting plate using short aluminum or stainless steel, threaded standoffs. A flanged outer enclosure will fit over the top of the CCA stack and will be affixed to the mounting plate using screws. Lateral support for the CCA stack will be provided by structure added to the enclosure as the vertical standoffs are not expected to provide enough strength against lateral loading.

Anticipated modifications to the mounting plate include four CCA mounting holes, and three or four holes along each edge of the mounting area for securing the enclosure.

Again, the location and orientation of this payload on the HASP structure is flexible.

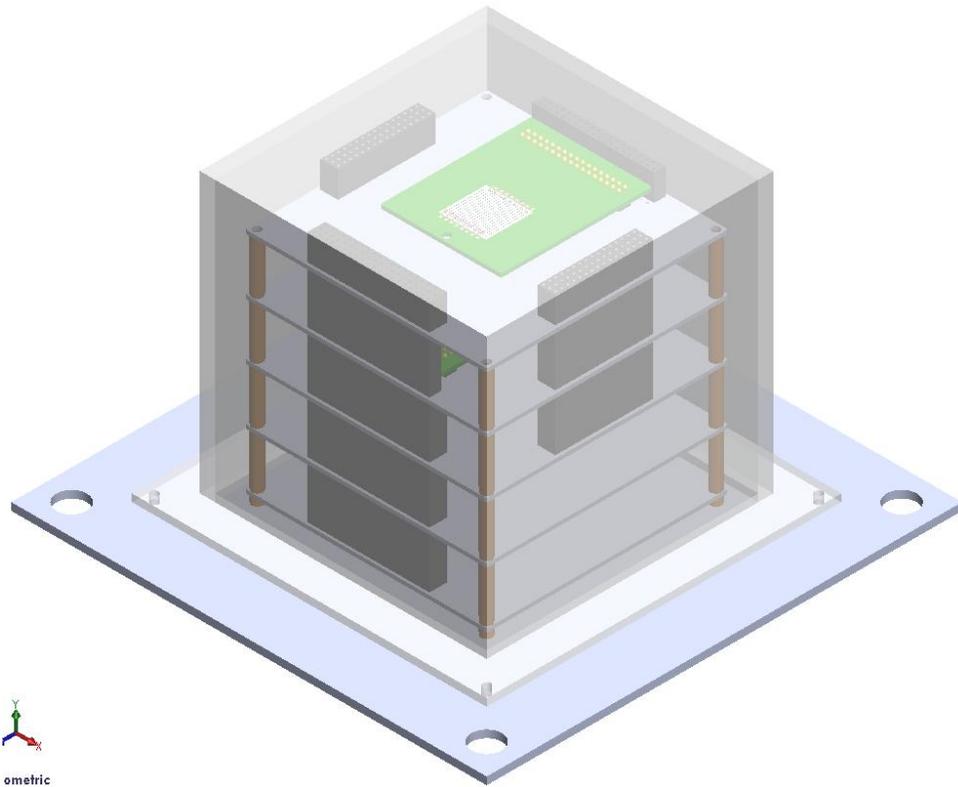


Figure 10: Isometric view of payload electronics stack and enclosure attached to HASP mounting plate.

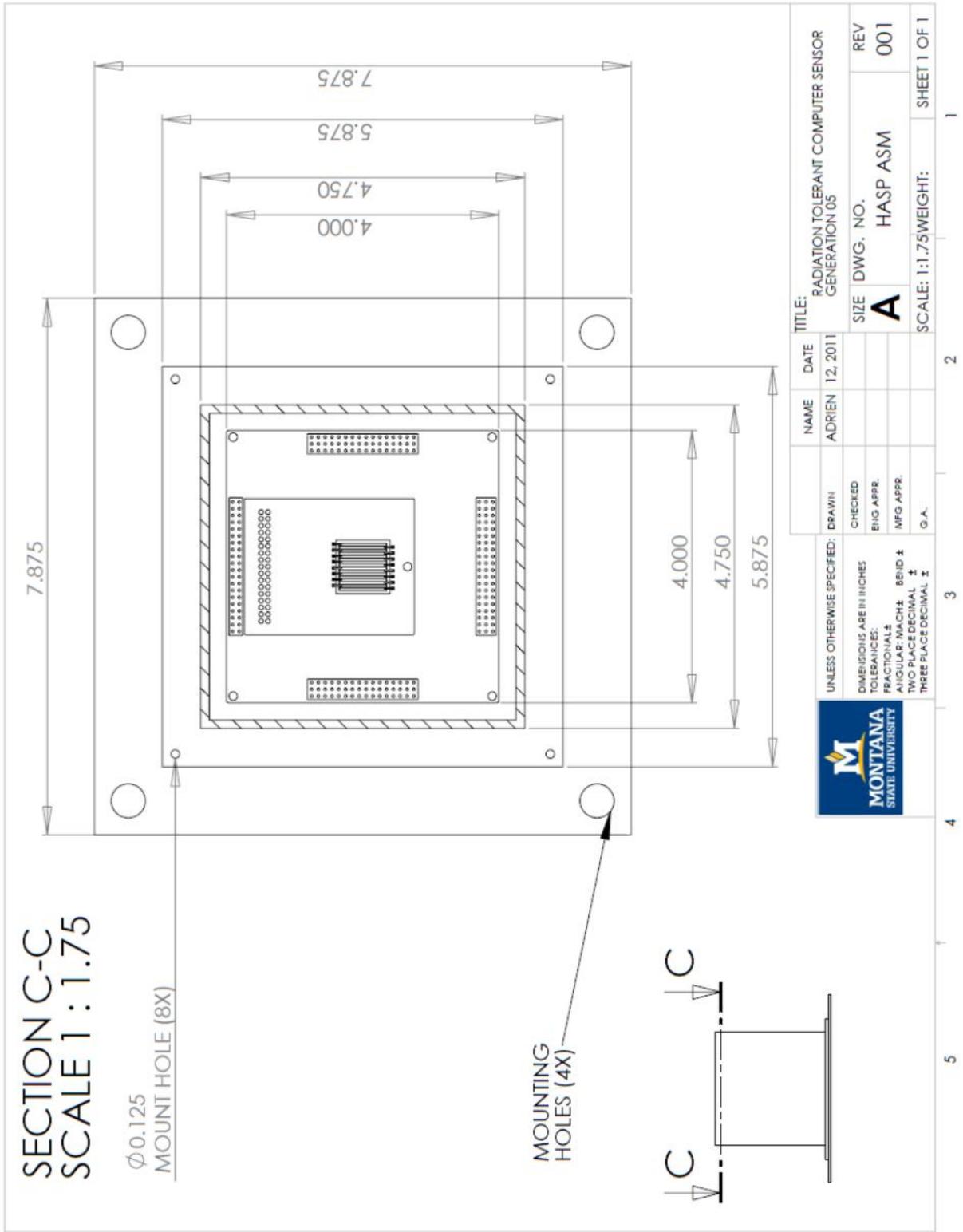


Figure 11: Top view of payload with electronics stack. Dimensions are in inches.

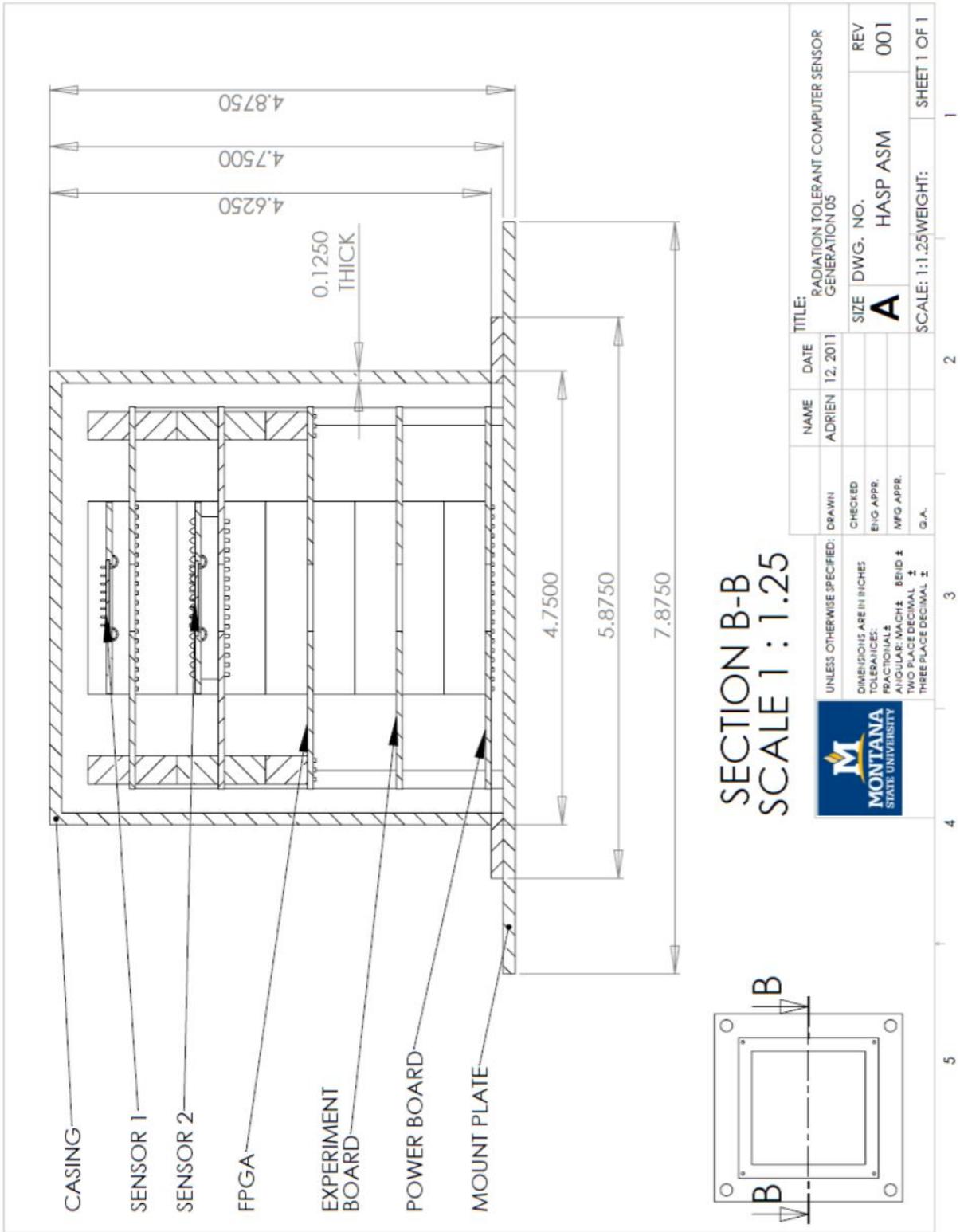


Figure 12: Side view of payload electronics stack. Dimensions are in inches.