May HASP status report from the SKC Wide Field Camera team

The focus for May was readying the SKC payload for the May 26th preliminary thermal/vac test at Palestine. The main milestones/issues that arose during May before thermal/vac:

- The interface PCB design was finalized, and the board was ordered and received. We can load our configuration and C code on the FPGA and control the camera via the serial interface. For the preliminary thermal/vac test the control code was written to allow the test team to control the camera by using a laptop connected to the camera interface board via a RS232 cable. Through this interface the image detector chip can be pit into a low power suspend mode, put into a mode of acquiring frames continually at 15 frames/second, a frame can be written to SRAM upon command, and a thumbnail of the frame stored in SRAM can be retrieved via serial upon command. An issue with the FPGA configuration used for the thermal/vac test is the read of the pixel data from the image detector IC is controlled in our C code rather than directly in hardware on the FPGA. This has turned out to be inadequate as the FPGA clock doesn't run fast enough to keep up with the pixel clock, and this results in missing the data from some of the pixels and so yields a corrupted image. The new FPGA configuration will implement a direct routing of the pixel data to SRAM. This will allow for a pixel clock of up to 12.5 MHz. The detector chip yields valid image data as long as the pixel clock is over 6 MHz. The new VHDL configuration should be up and running this coming week.

- The payload housing and lens baffle were constructed from anodized aluminum, and the headboard and interface board were mounted inside the housing. No insulation was added inside the payload housing before thermal/vac. Metal strips were added to conduct heat from the heat-generating components on the boards to the housing. These heat-conducting strips were removed in Palestine before thermal/vac on the advice of Don from the CSBF as being unnecessary for the amount of heat our payload generates (the current draw is about 0.11 A @ 30 V $\Rightarrow$ 3.3 W).

The SKC preliminary thermal/vac test team consisted of three students (Matt Friedlander, Brad Lehuta, and Sean Shriner) and one faculty mentor (Thomas Trickel). They were assisted during the May 26th test by Don, Tom, and Robert from the CBSF. The main information gained from the May 26th thermal/vac test:

- During thermal/vac the SKC payload was first taken to cold temperatures. At -37°C and 600 mbar serial communication with the payload was lost. The chamber was reheated and opened, and the FPGA needed to have its configuration reloaded to restore function. Don pointed out the chamber temperature is lower at the bottom of the chamber than indicated on the chamber thermometer. He also recommended soldering the FPGA oscillator onto the board instead of socketing it. The oscillator was soldered in and the payload was placed higher in the chamber for a cold soak retest. The payload was then operated successfully at -30°C and 1 mbar for one hour before serial communication was lost again. On reheating the FPGA the configuration needed to be reloaded to restore function. The payload was then taken to +30°C and 600 mbar for one hour, and then 50°C and 600 mbar for 20 minutes, with the payload operating successfully throughout. After the hot soak test the CSBF work day had ended and no further testing was done.

- After observing the performance of our payload during thermal/vac Don recommended for flight that we don't heat sink our ICs to the housing and baffle, and we should pack the PCBs in insulation and make the housing more reflective. Without the need of a radiator we will paint the baffle and housing white and also wrap it in Mylar to reduce the level of heating from the Sun. We will make these changes to our thermal system for the August thermal/vac.