Salish Kootenai College January status report:

This report will address the reviewer comments about our 2010 HASP payload proposal.

Reply to comments:

1a and comment 2.
Revised drawings demonstrate the payload is now appropriately positioned on the mounting plate and no longer violates the keep out area.

The revised drawings are attached.

1b.
Mass Budget:

DB9 (male) <0.029 kg	Measured with excess wire mass
DB9 (female) 0.008	Measured
EDAC (male) ~ 0.04	Roughly estimated based on measurements
EDAC (female) ~ 0.017	of objects of comparable size.
Voltage regulator 0.005 kg	Measured
PCB w/ chipset & sockets ~0.07 kg	This is based on the measured weight of a stamp available in our Lab that is comparable in size and has a similar chipset.
Enclosure ~0.114 kg Baffle ~0.202 kg	These mass calculations are based on the vendor's approximation of 1 lb/sq.ft. <basiccopper.com/thicknessguide.html> for 22Mil Cu, and an approximated cumulative area requirement of 25.4cm x 25.4cm = 645.16cm^2.
Payload to mounting plate fasteners ~0.022 kg	Based on 5mm d x 16mm l bolt/washer/nut combination of 5.5g ea. x 4 points
Camera Lens ~0.005 kg	Based on the measured weight of a lens similar to the one to be implemented.

Total ~ 0.512 kg

1c.
The team has remaining questions for this section; namely, the connection style to our board. We have reviewed the HASP Student Payload Interface Manual and we are unclear if the DB9 and EDAC 516 connectors are on both ends of the pigtail connection. We would like to know if the connectors are male or female, and more specifically the terminal pin style on the EDAC 516 connector.

1d.
Xilinx Virtex-6 FPGA

Voltage	2.5V
Power Consumption	1W
Temperature range (–65°C to +150°C)	

Micron MT9M131 CMOS Megapixel Digital Image Sensor

Voltage	2.5V
Power Consumption	0.1W
Operating temperature –30 °C to +70 °C	

Xilinx Virtex 6 FPGA will be used a soft-core processor running a version of Linux. RAM and FLASH memory operations for the Camera system will be controlled by the Xilinx Virtex - 6 FPGA. The Micron MT9M131: SOC Megapixel Digital Image Sensor operations during flight conditions will be controlled by the FPGA. The FPGA will implement a JPEG thumbnails utility so the SKC HASP team can receive periodic images from the camera via the HASP upload link.

Flash memory chip: MT29F8G08AAAWP-ET:A TR

Voltage	3.3V
Power Consumption	0.1W
Operating temperature -40 °C to +85 °C	

This micron flash memory chip has 8 gigabytes of storage capacity.

Voltage regulators

Power Consumption	0.3W

This brings our baseline power budget to 1.5 Watts.

1e.
The baseline thermal design is to dissipate heat generated by the payload electronics (FPGA, image detector, FLASH memory, and voltage regulators). A metal strip in thermal contact with the top of each heat-generating component runs from the chip to the lens baffle, which acts as a radiator. Arctic Silver 5 thermal grease compound was selected as the adhesive to bind the conductive strips to the chips

and the baffle. This compound was selected for its high-density metal content. The high metal content conducts heat more efficiently then standard ceramic based thermal grease compounds. The strips will be additionally secured to the chips with an overlaying metal plate that will be secured to the camera body and baffle.

1f.
The basline design for system control is a Xilinx FPGA from the Virtex-6 family. We have not yet selected a specific FPGA from that family. The FPGA will be run as a soft-core processor running with Linux as the operating system. The FPGA controls the operation of the image detector and the transfer of image data from the image detector to flash memory. We have selected a Micron Aptina MT9M131 image detector. This detector utilizes a Bayer pattern filter to generate color images. We have selected the Micron 8GB MT29F8G08AAAWP flash memory chip to store the image data acquired during the flight.

A block diagram will be attached as well.

1g.
The only data collected by this instrument is the image data. Two alternatives are being considered for the data format for flash memory storage: raw images or JPEG compressed. The trade is between reducing the size of stored images vs. the processing needed to perform onboard JPEG compression.
We anticipate the need to occasionally downlink small thumbnail images to verify camera operation. (a 37 KB thumbnail no more than once every 5 minutes).

1h and comment 4.
We don't need to send an uplink command every minute, only a few times an hour. Baseline uplink control commands include, payload control system reboot, adjust exposure time, adjust exposure frequency, thumbnail downlink request.
Uplink control format: 3 Bytes for specifying which command (leaves a margin for 4 additional commands to be added to the command list), 5 Bytes for command parameters
(5 Bytes gives 32 discrete parameter values, e.g. 32 exposure times)

1i.
Early February purchase FPGA and image detector board.
Feb – March: circuit board design, FPGA programming.
April – May: payload assembly and in-house testing
End of May: thermal vac testing at CSBF.
June: perform needed design modifications indicated from or by thermal vac testing.
July: perform additional in-house testing of modified design.
Early August: payload integration.
September: payload flight.

1j.
We anticipate three students and one faculty mentor will need to travel to Palestine TX for integration.

Matt Friedlander: Test and operations lead.
Kody Ensley: Project management lead.
Sean Shriner: Design lead.
Tim Olson: Faculty mentor.

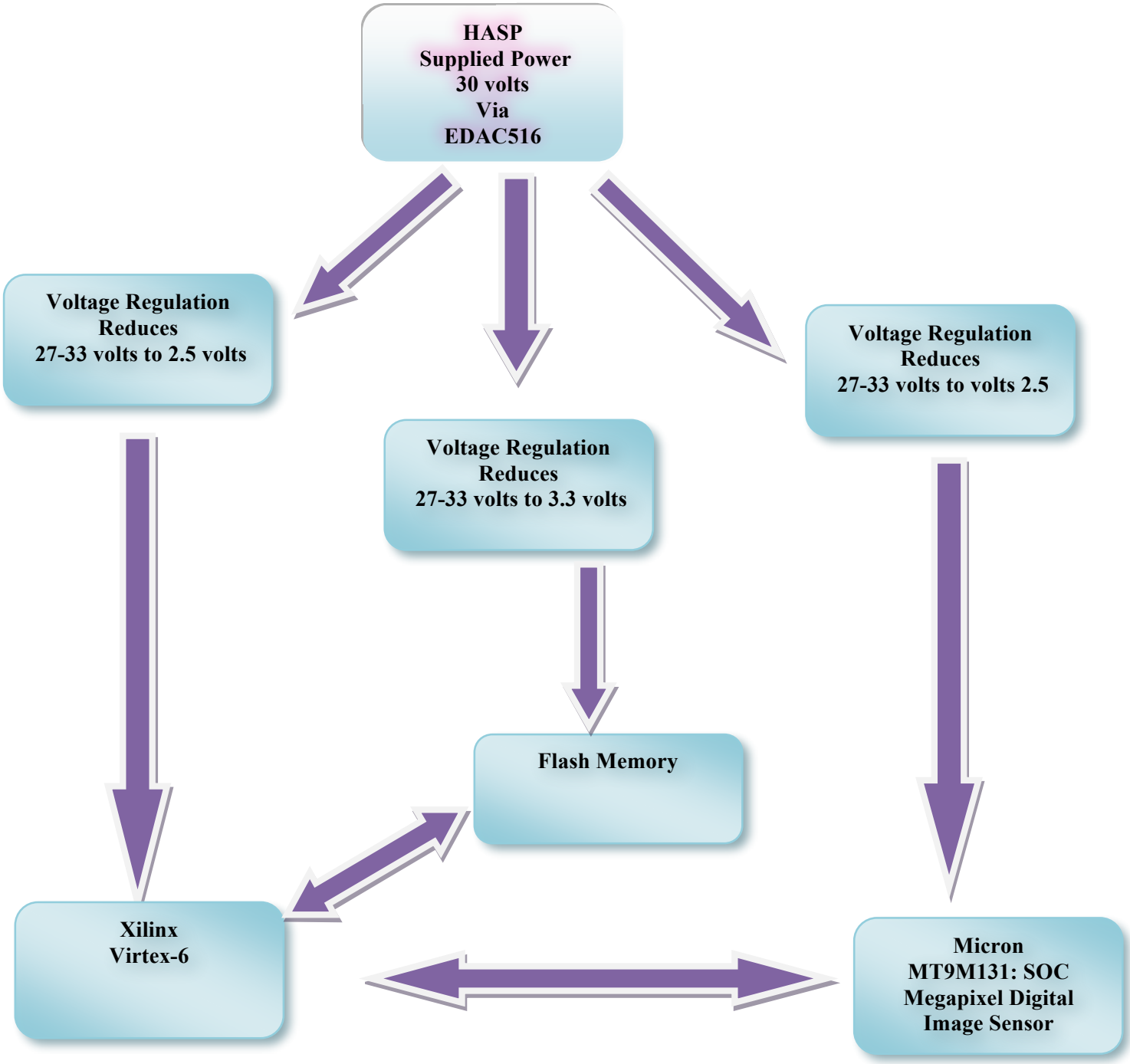
The integration team will be verifying correct operation of the payload once the payload is integrated with the HASP platform. This verification will consist of the acquisition of images and the successful storage and retrieval of these images from flash storage.

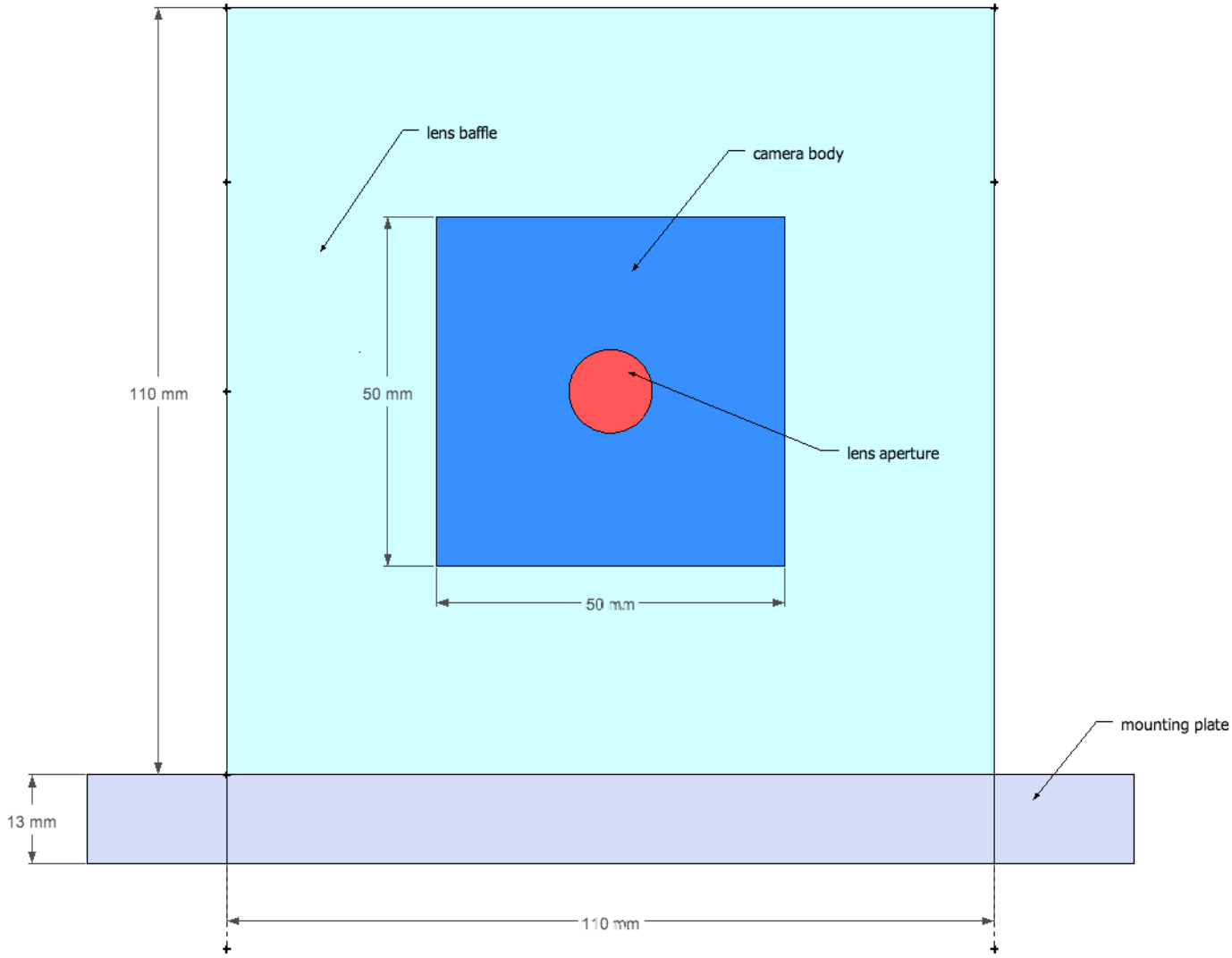
1k.
We anticipate three students and one faculty mentor will be needed for flight operations.

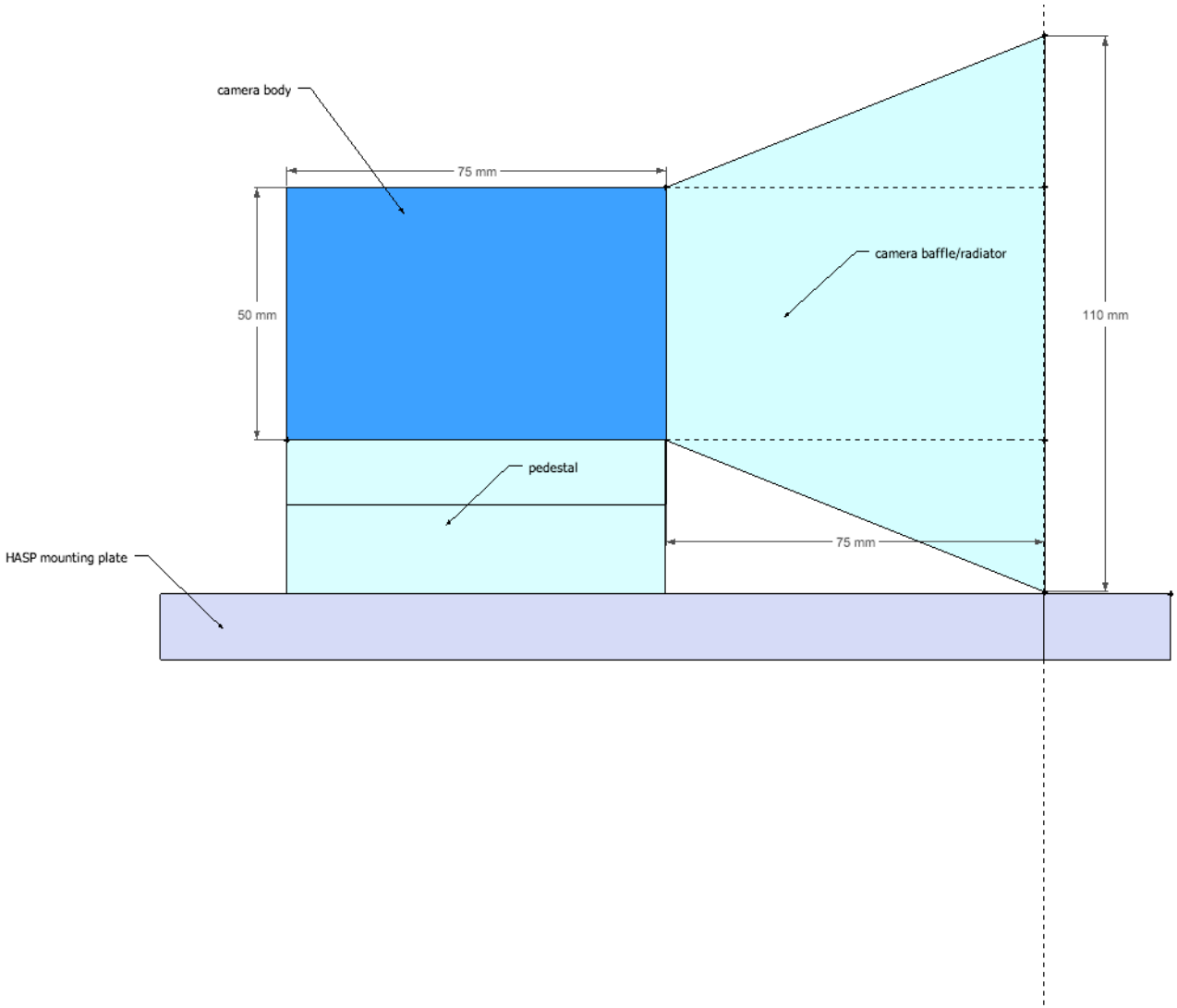
Matt Friedlander: Test and operations lead.
Kody Ensley: Project management lead.
Sean Shriner: Design lead.
Tim Olson: Faculty mentor.

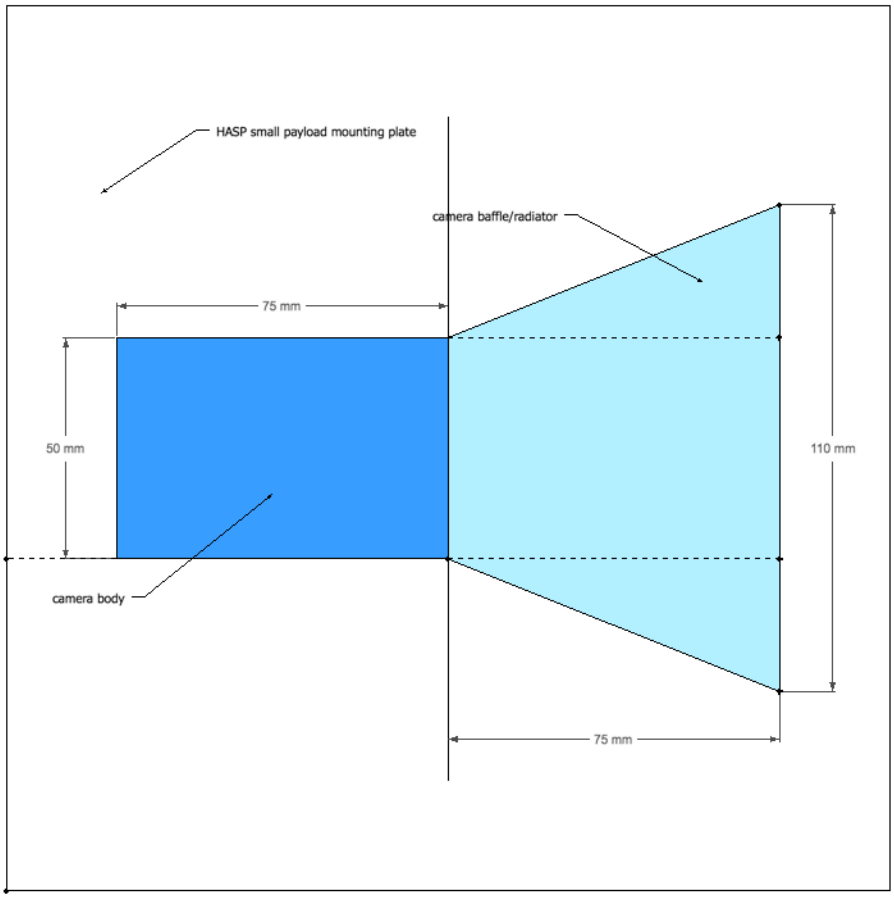
Only the operations lead (Friedlander) will request uplink commands to be sent by the HASP operator.
The other three team members will assist the operations lead in the analysis of downlinked thumbnail images and determination of the need to change image exposure time and frequency.

5.
Faculty mentor Olson will ask Bert Knighton if he is willing to serve as an additional mentor to our team.


HASP
Supplied Power
30 volts
Via
EDAC516
Voltage Regulation
Reduces
27-33 volts to 2.5 volts
Voltage Regulation
Reduces
27-33 volts to 3.3 volts
Voltage Regulation
Reduces
27-33 volts to volts 2.5
Flash Memory
Xilinx
Virtex-6
Micron
MT9M131: SOC
Megapixel Digital
Image Sensor


lens baffle
camera body
110 mm
50 mm
lens aperture
50 mm
mounting plate
13 mm
110 mm


camera body
75 mm
50 mm
camera baffle/radiator
110 mm
pedestal
75 mm
HASP mounting plate


HASP small payload mounting plate
camera baffle/radiator
75 mm
50 mm
110 mm
camera body
75 mm