Salish Kootenai College February status report:

Hello from Salish Kootenai College.

Completed objectives:

- We have received our image detector chip and evaluation board and have begun work testing the image modes in varying lighting conditions.

- We have decided to use the camera headboard as shipped instead of building a headboard from scratch as the shipped headboard meets our requirements.

- The image detector chip came with an F/2 lens, while our baseline design called for a F/1.2 lens. We are testing with the F/2 lens to see if it will meet our requirements for field of view. The lens holder is compatible with lenses from several vendors, and we plan on buying other lenses to compare against the in hand F/2 lens.

- We have decided to use a DB9 connector to mate the pigtail communication line to our project. We have not yet decided what connector we will use to mate to the power pigtail lines. One reason we have not yet selected a power connector type is the unknown diameter of the power pigtail cables.

- The camera headboard will be attached to the front plate via four screws in each corner of the headboard. The control board will be mounted to the camera headboard from behind. The camera headboard comes with a 2x13 header connector, as such we have opted to use a mating 2x13 header for interconnection to the control board. The control board will be attached via bolts and standoffs to the same four screw points on the camera headboard. This will create a robust connection for the interconnection between the camera headboard and the control board as well as a strong mounting point to the chassis.

- One change in our baseline design has been the switch from a Xilinx FPGA to an Altera FPGA. The primary reason for the change in FPGA was the unavailability of the Xilinx Spartan 6 and Virtex 6 for 8 weeks. We considered using older technologies such as the Spartan 4 and the Virtex 4, however the older Xilinx FPGAs have a significantly higher current consumption.
Additionally we already have a working knowledge of Altera FPGA's and the accompanying development software. We will be performing our original development on an Altera DEII development board, which features a Cyclone II FPGA; we will most likely fly a Cyclone III FPGA.
We initially chose the Xilinx FPGA's because of the devices radiation tolerant design. Altera does not have a product they advertise as space rated. However, Altera has taken steps in the design of the Cyclone III to prevent radiation upsets.
See below link for more information.
http://www.altera.com/support/devices/reliability/seu/seu-index.html

- We have attached a preliminary layout for the controller board. We are currently working on a complete schematic.

- We have completed a power subsystem schematic and have attached it to the end of this document. The power subsystem has been implemented using DC-to-DC converters that take the HASP supplied 30V to 5V. The DC-to-DC converter is a PXB15-48WS05.

- Also attached you will find the schematic for the camera headboard.

Current objectives:

Software:

- Our current approach for the design of the controlling software is an interrupt driven task-switching approach. Specific tasks would have a level of importance assigned to them so that more important tasks are allowed to finish uninterrupted.

- We have opted to use an open source I2C core in our FPGA VHDL model. This I2C core will allow us to generate the proper signals in order to communicate with the camera headboard. The I2C open core uses a Wishbone interconnection whereas the Altera NIOS CPU utilizes an Avalon interconnection. Currently we are working on the interface between the I2C open core and the Altera NIOS CPU.

- For the development of the I2C driver code, we have opted to start development on the Teensy++ microcontroller. The Teensy++ features an Atmel AT90USB128 microprocessor, which uses a version of C closely related to the Altera development language. We have extended experience with the Teensy++ and have a version of the I2C communication protocol constructed from previous projects. This will allow us to quickly test and implement the driver code once we have completed work on the I2C open core interface.

Flash Storage:

- We have two options of how to attach our flash storage.

- Soldering the flash storage directly to the controller board would create a robust connection. However, this approach would require engineering a separate subsystem for retrieval of data.

- Soldering a receptacle to the board for SD flash cards is our second option. This creates a method to retrieve our data almost instantly, without the need

to develop a separate subsystem. The drawback to this approach is the potential for the SD card to become dislodged in flight.

Thermal subsystem:

- We would like to have all of our components hooked up and running in order to measure a final current draw. Once we have the final power dissipation calculation we will move ahead with the radiator design.
One student has been actively researching materials with high emissivity for the camera housing and underside radiator so we can quickly make a selection when we are ready.

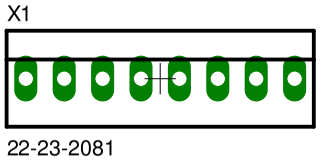
- After speaking with Berk Knighton, we have implemented a few of his suggestions.

- We are currently designing a series of temperature sensors to be outfitted to our heat producing devices. These sensors will automate a power reduction mode or a sleep mode in our program if a device starts to overheat. Once the components have had a chance to cool down we would wake the devices.

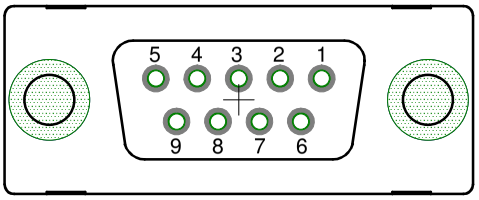
- Berk Knighton also suggested we add an additional radiator to the underside of our project. This additional radiator would be out of direct sunlight for part of our mission and helps keep the size of the topside radiator components down.
  One question we have is how much space do we have for the underside radiator?
  Do we have access to the same dimensions of 15cm x 15cm x 30cm?

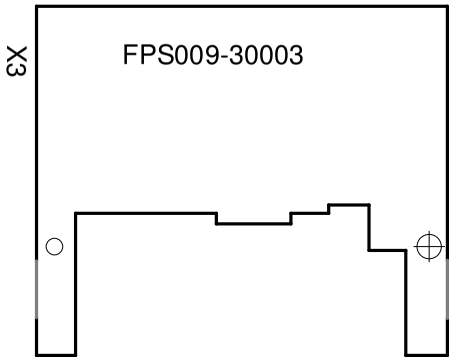
-2010 Salish Kootenai College HASP Team

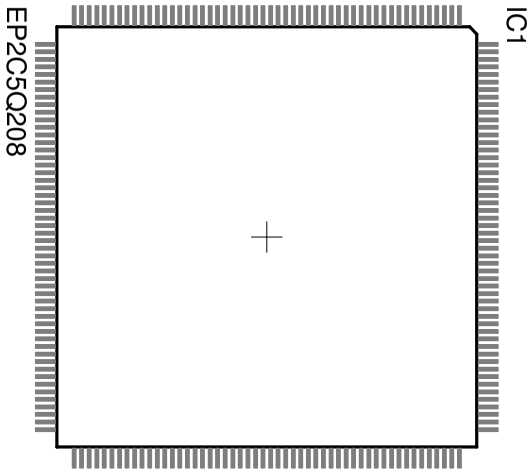
HASP Power Connector



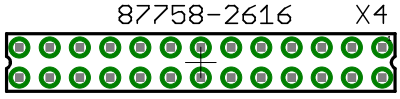
X2

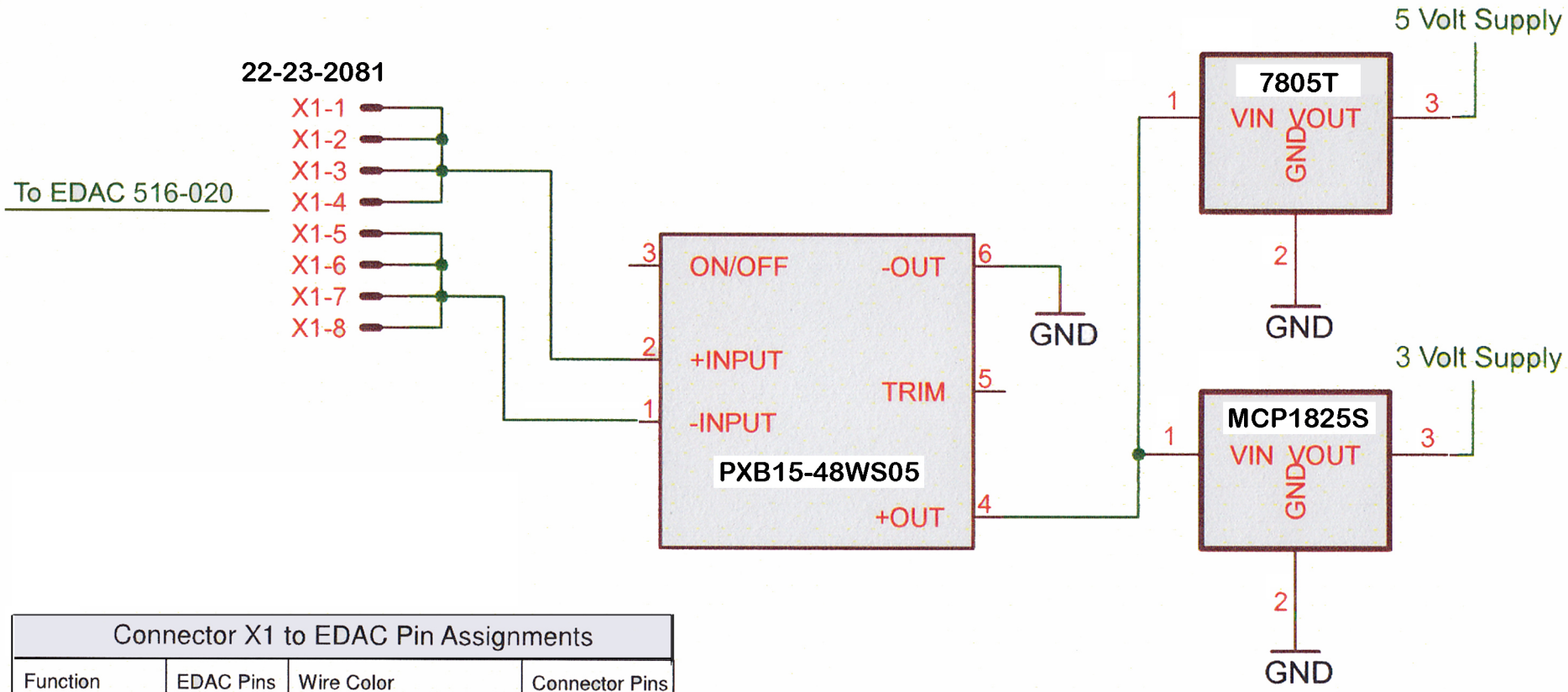






Camera Headboard Connector





Connector X1 to EDAC Pin Assignments			
Function	EDAC Pins	Wire Color	Connector Pins
+30vDC	A, B, C, D	White with Red Stripe	1, 2, 3, 4
Power Ground	W, T, U, X	White with Black Stripe	5, 6, 7, 8

Salish Kootenai College
Computer Engineering Department

SKC Wide Field Camera
Power Subsystem
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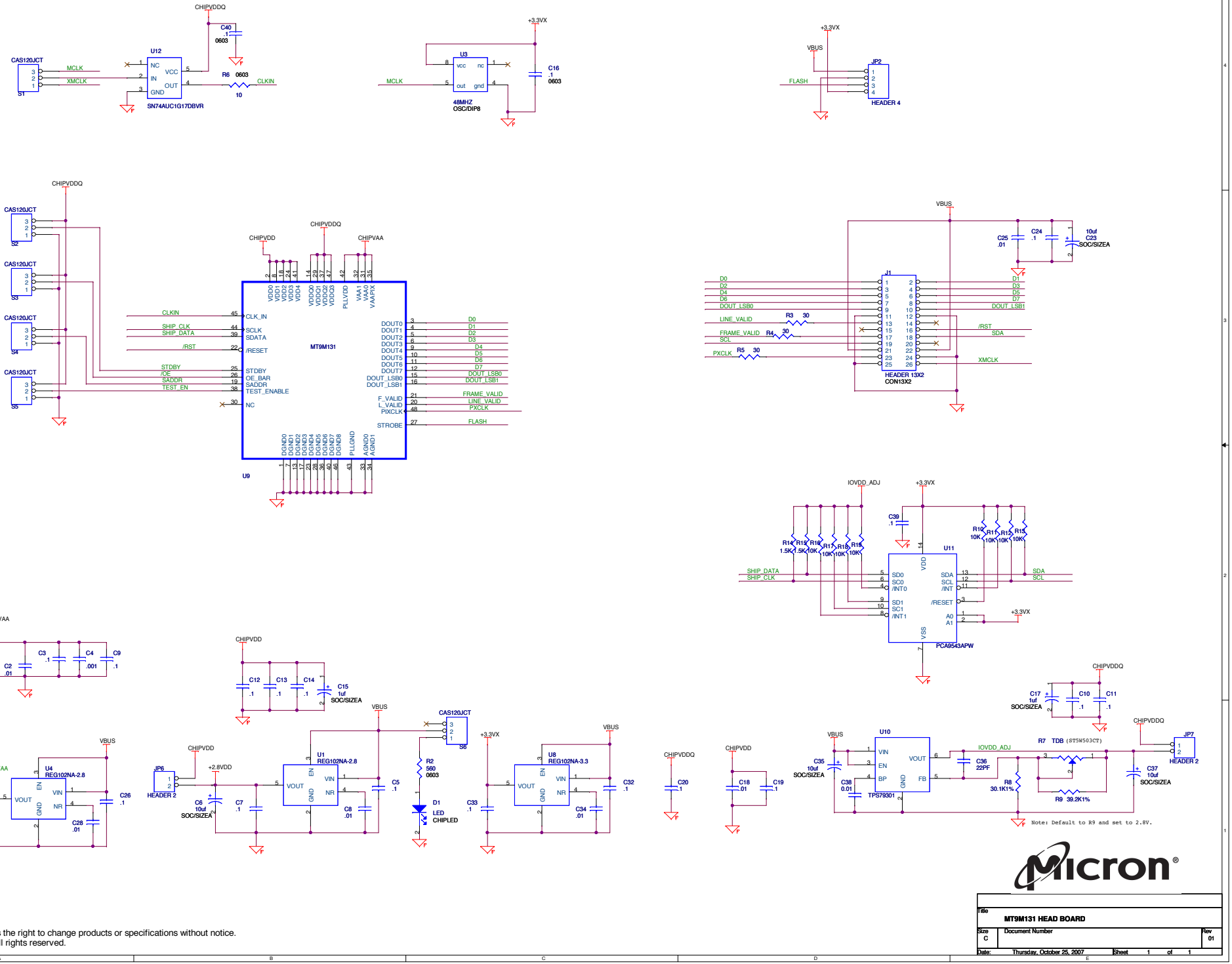

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Size C	Document Number	Rev 01
Date: Thursday, October 25, 2007	Sheet 1 of 1	